Test #2 Take Home Extension - Due Wed, August 1st, Noon.

Because of the poor results on test #2, I am going to allow you to take it home and rework problems #1, #4, #5, and #6. You will be able to recover any points lost on these problems by submitting to me correct solutions AND Vhdl/Verilog code/simulation results that back up your statements. You cannot recover points lost on problems #2, #3.

This will be due on Wednesday, August 1st. There will be NO final examination -- only two exams plus the simulations.

Special Instructions :

> For problem #1, the p1.zip file has two VHDL libraries -- 'gcmos' and 'test2'. The *gcmos* library is a very small cell library -- these are the models you need to modify to satisfy the requirements of problem #1 (you cannot add any extra ports on the entities). The test2 library contains two sample netlists (dec3to8 and firl0p0). You will need to write two testbenches that instantiates these designs and which will display the cell count of these designs as specified in Problem #1 (you don't have to actually exercise the ports on the designs in any meaningful manner in your testbenches).

You must turn all of your work over to me complete with Makefiles, testbenches, and all code that demonstrates support for your answers (use a ZIP or compressed tar file). You MUST supply me with instructions that says exactly how to compile the code for the individual solutions, and how to run the models. If you fail to supply me with this information, then I will not grade the solutions.

Simulation #6 -- due Friday, July 27 - Noon.

For Simulation #6, download the ZIP archive for the matrix example for Synopsys Behavorial compiler, and modify the model such there are individual input ports labeled X,Y,Z,W . Do a minimum resource implementation and a maximally pipelined implementation (initiation rate = 1). Modify the testbenches to accommodate the new ports. You will still need to input the matrix coefficients - do this over port X.