Q68HC05xx

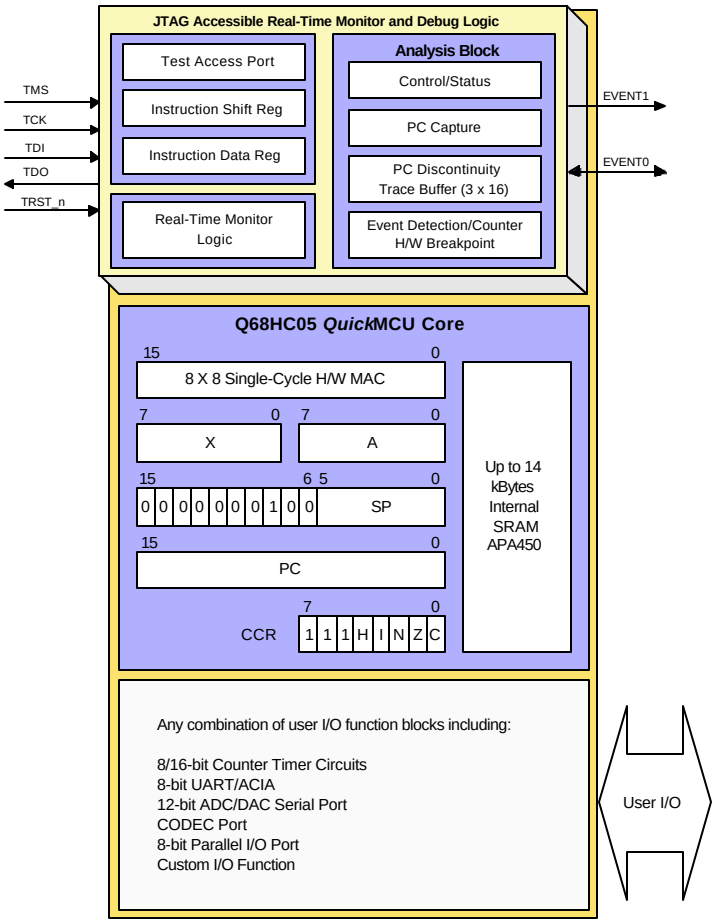
FPGA-Embeddable
Microcontroller Soft Core

Features

- 100% 68HC05 machine and source code compatible Verilog microcontroller soft core.
- Pipeline architecture executes many instructions at least two times faster than the industry standard 68HC05.
- 24.5 MHz (12.25 MIPS) operation when implemented in an ACTEL ProASIC^{PLUS}.
- Optional 8 X 8 unsigned multiply and accumulate in just 40ns at 50MHz.
- Up to six separate interrupt request inputs, each with its own vector.
- Total of 3 to 14 kbytes of internal program/data RAM (APA075 - APA450 respectively).
- Up to 64k bytes of external addressing. Optional Extended Addressing circuit extends address reach to 4 mega bytes.
- Core and peripherals available in synthesizable Verilog RTL, Verilog netlist, or Schematic level format.
- On-chip JTAG accessible real-time debug logic module enables on-the-fly examination and editing of programs and data with zero software overhead.
- Compatible with Domain Technologies BoxView high level language debugger and JTAG controller pods, and both Byte Craft and COSMIC C compiler.
- Low cost, royalty-free, Q68HC05xx Verilog netlist library license includes QuickCores Q68HC05xx CPU, PIO, PIO with key wake-ups, counter/timer circuit, asynchronous serial communications interface, extended addressing circuit, various sizes of RAM blocks, example top level design Verilog source code, .S19 to .v conversion utility, example Verilog test fixture and BoxView C Language Source Level Debug software for use with QuickCores MUSKETEER^{TM}.

24.5 MHz Q68HC05xx *Quick*MCU^{TM}

(ACTEL ProASIC^{PLUS} Implementation)



General Description

The Q68HC05xx *Quick*MCU is the industry's first internet-downloadable microcontroller core that can be programmed directly into a QuickCores MUSKETEER re-programmabl IP delivery system using BoxView's integrated STAPL player. The QuickCores Q68HC05 QuickMCU is built on QuickCores patented real-time monitor architecture which allows monitoring and debugging of embedded applications in real-time using zero software overhead on the target side.

Further architectural enhancements of the QuickCores Q68HC05 over the industry standard version of 68HC05 include an optional 8 x 8 single-cycle hardware multiply instruction, relocatable stack and vector base address, and a three-stage instruction pipeline which eliminates at least one clock per op-code off instruction execution cycle times.

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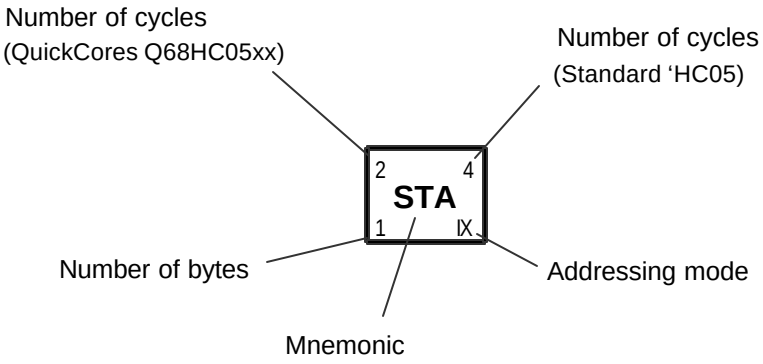
www.quickcores.com

Q68HC05xx Op-Code Map

			Branch	Read-Modify-Write					Control		Register-Memory					
	DIR	DIR	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX
	MSB 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
LSB 0	4 5 BRSET0 3 DIR	4 5 BSET0 2 DIR	2 3 BRA 2 REL	5 5 NEG 2 DIR	1 3 NEGA 1 INH	1 3 NEGX 1 INH	5 6 NEG 2 IX1	5 5 NEG 1 IX	8 9 RTI 1 INH		2 2 SUB 2 IMM	3 3 SUB 2 DIR	4 4 SUB 3 EXT	4 5 SUB 3 IX2	3 4 SUB 2 IX1	2 3 SUB 1 IX
1	4 5 BRCLR0 3 DIR	4 5 BCLR0 2 DIR	2 3 BRN 2 REL						5 6 RTS 1 INH		2 2 CMP 2 IMM	3 3 CMP 2 DIR	4 4 CMP 3 EXT	4 5 CMP 3 IX2	3 4 CMP 2 IX1	2 3 CMP 1 IX
2	4 5 BRSET1 3 DIR	4 5 BSET1 2 DIR	2 3 BHI 2 REL		1 11 MUL 1 INH						2 2 SBC 2 IMM	3 3 SBC 2 DIR	4 4 SBC 3 EXT	4 5 SBC 3 IX2	3 4 SBC 2 IX1	2 3 SBC 1 IX
3	4 5 BRCLR1 3 DIR	4 5 BCLR1 2 DIR	2 3 BLS 2 REL	5 5 COM 2 DIR	1 3 COMA 1 INH	1 3 COMX 1 INH	5 6 COM 2 IX1	5 5 COM 1 IX	10 10 SWI 1 INH		2 2 CPX 2 IMM	3 3 CPX 2 DIR	4 4 CPX 3 EXT	4 5 CPX 3 IX2	3 4 CPX 2 IX1	2 3 CPX 1 IX
4	4 5 BRSET2 3 DIR	4 5 BSET2 2 DIR	2 3 BCC 2 REL	5 5 LSR 2 DIR	1 3 LSRA 1 INH	1 3 LSRX 1 INH	5 6 LSR 2 IX1	5 5 LSR 1 IX	RESRVD		2 2 AND 2 IMM	3 3 AND 2 DIR	4 4 AND 3 EXT	4 5 AND 3 IX2	3 4 AND 2 IX1	2 3 AND 1 IX
5	4 5 BRCLR2 3 DIR	4 5 BCLR2 2 DIR	2 3 BCS/BLO 2 REL								2 2 BIT 2 IMM	3 3 BIT 2 DIR	4 4 BIT 3 EXT	4 5 BIT 3 IX2	3 4 BIT 2 IX1	2 3 BIT 1 IX
6	4 5 BRSET3 3 DIR	4 5 BSET3 2 DIR	2 3 BNE 2 REL	5 5 ROR 2 DIR	1 3 RORA 1 INH	1 3 RORX 1 INH	5 6 ROR 2 IX1	5 5 ROR 1 IX			2 2 LDA 2 IMM	3 3 LDA 2 DIR	4 4 LDA 3 EXT	4 5 LDA 3 IX2	3 4 LDA 2 IX1	2 3 LDA 1 IX
7	4 5 BRCLR3 3 DIR	4 5 BCLR3 2 DIR	2 3 BEQ 2 REL	5 5 ASR 2 DIR	1 3 ASRA 1 INH	1 3 ASRX 1 INH	5 6 ASR 2 IX1	5 5 ASR 1 IX		1 2 TAX 1 INH		3 4 STA 2 DIR	4 5 STA 3 EXT	4 6 STA 3 IX2	3 5 STA 2 IX1	2 4 STA 1 IX
8	4 5 BRSET4 3 DIR	4 5 BSET4 2 DIR	2 3 BHCC 2 REL	5 5 A/LSL 2 DIR	1 3 A/LSLA 1 INH	1 3 A/LSLX 1 INH	5 6 A/LSL 2 IX1	5 5 A/LSL 1 IX	RESRVD	1 2 CLC 1 INH	2 2 EOR 2 IMM	3 3 EOR 2 DIR	4 4 EOR 3 EXT	4 5 EOR 3 IX2	3 4 EOR 2 IX1	2 3 EOR 1 IX
9	4 5 BRCLR4 3 DIR	4 5 BCLR4 2 DIR	2 3 BHCS 2 REL	5 5 ROL 2 DIR	1 3 ROLA 1 INH	1 3 ROLX 1 INH	5 6 ROL 2 IX1	5 5 ROL 1 IX	RESRVD	1 2 SEC 1 INH	2 2 ADC 2 IMM	3 3 ADC 2 DIR	4 4 ADC 3 EXT	4 5 ADC 3 IX2	3 4 ADC 2 IX1	2 3 ADC 1 IX
A	4 5 BRSET5 3 DIR	4 5 BSET5 2 DIR	2 3 BPL 2 REL	5 5 DEC 2 DIR	1 3 DECA 1 INH	1 3 DECX 1 INH	5 6 DEC 2 IX1	5 5 DEC 1 IX	RESRVD	1 2 CLI 1 INH	2 2 ORA 2 IMM	3 3 ORA 2 DIR	4 4 ORA 3 EXT	4 5 ORA 3 IX2	3 4 ORA 2 IX1	2 3 ORA 1 IX
B	4 5 BRCLR5 3 DIR	4 5 BCLR5 2 DIR	2 3 BMI 2 REL						RESRVD	1 2 SEI 1 INH	2 2 ADD 2 IMM	3 3 ADD 2 DIR	4 4 ADD 3 EXT	4 5 ADD 3 IX2	3 4 ADD 2 IX1	2 3 ADD 1 IX
C	4 5 BRSET6 3 DIR	4 5 BSET6 2 DIR	2 3 BMC 2 REL	5 5 INC 2 DIR	1 3 INCA 1 INH	1 3 INCX 1 INH	5 6 INC 2 IX1	5 5 INC 1 IX	RESRVD	1 2 RSP 1 INH		2 2 JMP 2 DIR	3 3 JMP 3 EXT	3 4 JMP 3 IX2	2 3 JMP 2 IX1	2 2 JMP 1 IX
D	4 5 BRCLR6 3 DIR	4 5 BCLR6 2 DIR	2 3 BMS 2 REL	4 4 TST 2 DIR	1 3 TSTA 1 INH	1 3 TSTX 1 INH	4 5 TST 2 IX1	4 4 TST 1 IX	RESRVD	1 2 NOP 1 INH	5 6 BSR 2 IMM	5 5 JSR 2 DIR	6 6 JSR 3 EXT	6 7 JSR 3 IX2	5 6 JSR 2 IX1	5 5 JSR 1 IX
E	4 5 BRSET7 3 DIR	4 5 BSET7 2 DIR	2 3 BIL 2 REL						1 2 STOP 1 INH		2 2 LDX 2 IMM	3 3 LDX 2 DIR	4 4 LDX 3 EXT	4 5 LDX 3 IX2	3 4 LDX 2 IX1	2 3 LDX 1 IX
F	4 5 BRCLR7 3 DIR	4 5 BCLR7 2 DIR	2 3 BIH 2 REL	5 5 CLR 2 DIR	1 3 CLRA 1 INH	1 3 CLRX 1 INH	5 6 CLR 2 IX1	5 5 CLR 1 IX	1 2 WAIT 1 INH	1 2 TXA 1 INH		3 4 STX 2 DIR	4 5 STX 3 EXT	4 6 STX 3 IX2	3 5 STX 2 IX1	2 4 STX 1 IX



Address Mode Abbreviations

DIR	Direct
IMM	Immediate
EXT	Extended
INH	Inherent
REL	Relative
IX	Indexed (no offset)
IX1	Indexed (8-bit offset)
IX2	Indexed (16-bit offset)

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