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Lab6: Transistor sizing

Introduction

The purpose of this lab is to introduce the concepts of transistor sizing – on how to arrive at transistor sizes for the pull-up and pull-down network of a logic gate, so as to get comparable rise and fall times and also minimize propagation delay.

Part A

Obtain the propagation delays 't_{plh}' (output going from low to high) and 't_{p_{hl}}' (high to low) for a CMOS inverter with the following aspect ratios: $W_n/L_n = 1.2/0.6$, $W_p/L_p = 1.2/0.6$ (all dimensions in microns).

Use a VDD of 3.3 volt. The inverter is driving a 100 fF load. Use a rise/fall time of 0.1ns for the input voltages.

Part B

Redesign the CMOS inverter of Part A so as to get comparable rise and fall times. Use minimum value of 1.2u for the NMOS width. The widths of the transistors can be varied in steps of lambda (lambda = 0.3u for the technology used for this lab).

Part C

Obtain the transistor sizes for the following logic gate, so as to get comparable rise and fall time:

$$F = \text{NOT} (D + A \cdot (B + C))$$

Also obtain the t_{plh} and t_{p_{hl}} values for the worst case input conditions, for the gate you designed driving a 100 fF load. You should first verify the functioning of your complex gate.

To turn in

1. t_{plh} and t_{p_{hl}} values for Parts A, B, C
2. The transistor sizes of the inverter for Part B
3. The transistor sizes for the logic gate of Part C (indicate the sizes on a schematic of the logic gate)
4. Mwave plots for the t_{plh} and t_{p_{hl}} measurement for the worst case inputs for Part C. Also show the output of the complex gate for all possible combinations of the inputs.

5. All spice files.