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ASIC Design and Manufacturing Requirements

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1 INTRODUCTION

1.1 Purpose

This document defines requirements for development of Application Specific Integrated Circuits (ASICs). It is intended to be used as an appendix to a Statement of Work.

The document complements the *ESA ASIC Design and Assurance Requirements* (AD1), which is a precursor to a future ESA PSS document on ASIC design. However, some requirements of AD1 has been included in this document for convenience reasons (AD1 still remains applicable).

Any deviations from these requirements require proper justification and ESA agreement before commencing the development. Requirements expressed or in a Statement of Work or similar document have precedence over this document.

1.2 Scope

The scope of this document is development of mainly digital ASICs of a quality suitable for space applications, where the developed devices shall be available as *Standard ASICs* as defined in Appendix B.

In case this document is used for the development of an ASIC not intended to become a *Standard ASIC*, which requirements are to be excluded should be agreed in writing before commencing the development.

Areas where this document might be applied in part are for the design and manufacturing of analog or mixed analog-digital ASICs, and for larger programmable logic devices such as FPGAs.

1.3 Applicable Documents

AD1 ESA ASIC Design and Assurance Requirements, QC/172/RdM Issue 1, June 1992
AD2 VHDL Modelling Guidelines, ASIC/001 Issue 1, September 1994
AD3 IEEE Standard VHDL Language Reference Manual, IEEE Std 1076-1993
AD4 IEEE Standard Multivalue Logic System for VHDL Model Interoperability (std_logic_1164), IEEE Std 1164-1993
AD5 Guidelines for the Preparation of ESA/SCC Detail Specifications, QCS/AJG/940806, August 1994

1.4 Reference Documents

RD1 Fault Coverage Measurement for Digital Microcircuits, Mil-Std 883D Method 5012.1, July 1990

2 DEVELOPMENT FLOW

This section contains additional and complementary requirements to those defined in AD1. The requirements applicable to each stage in the flow are specified, and the corresponding output is defined. The following stages have been defined:

- Design Initiation (Waived by default);
- Initial Analysis;
- Architectural Design;
- Detailed Design;
- ASIC Layout and Final Simulation;
- Prototype Manufacture and Test;
- Transfer of Design and Knowledge;
- Design Validation (Waived by default);
- ESA/SCC Qualification (Waived by default).

Each stage is intended to correspond to one or several distinct Work Packages (normally one Work Package per company involved).

Some stages have been marked as *Waived by default*. These stages have been included for the sake of completeness, and need only be executed if explicitly requested, e.g. in a Statement of Work.

2.1 General

Where possible, the contractor shall strive to achieve a certain overlap of the stages in order to decrease the development time, without decreasing the efficiency or increasing the risk for unnecessary work.

A particular stage and its corresponding Work Package(s) will be considered as completed when the associated output has been approved by ESA, and the corresponding Design Review has been successfully completed. A Design Review identifying a limited number of minor discrepancies can be completed after successful implementation of the identified corrective actions. A Design Review failing major acceptance criteria shall be repeated in full.

All design documentation, the VHDL model and the design database shall be subject to systematic version control, clearly identifying modifications between issues. It shall be ensured that obsolete data can not mistakenly be used, e.g. by always deleting all derived files after each modification of their source description.

Where surrounding components are referenced, e.g. for establishing requirements of external interfaces or for board-level simulation, European components shall be selected where possible.

No ASIC Design Initiation Document (ADID) or ASIC Control Plan as specified in AD1 need be established, unless explicitly requested.

2.2 Design Initiation (Waived by default)

This stage should normally have been performed before starting the ASIC development, and need only be performed if explicitly requested.

An ASIC Requirements Specification shall be established, defining all relevant system configurations and characteristics to a level allowing the device requirements to be derived. All system-level issues imposing requirements on the device shall be covered, such as system testing, power consumption, environment and system partitioning.

Thereafter the requirements on the device itself shall be established, in terms of functionality, operating modes, interfaces, performance, operating conditions etc.

The feasibility of the ASIC development shall be studied, based on foreseen development conditions, and be documented in the Feasibility Report. A risk analysis for the development shall also be included.

Output: ASIC Requirement Specification according to section 4.1;
Feasibility Report according to section 4.2.

2.3 Initial Analysis

If requested, this stage shall be included in the proposal for the ASIC development. In such case this stage need not be performed within the actual development.

In case no Functional Specification is provided, it shall be established in accordance with section 4.4. If the Functional Specification is provided, a critical review shall be performed, and incomplete or contradictory information shall be identified. In some cases an initial VHDL model might also be provided, and then the contractor shall review it for errors or discrepancies. The specification shall have precedence over a given model in case of discrepancies.

Since a device normally is used with derating w.r.t. its specifications, the requirements in the Functional Specification should be adjusted accordingly.

The baseline foundry, process and library to be used shall be selected, wherever possible selecting processes and libraries having - or being considered for - ESA/SCC Capability Approval. In case a route outside the ESA/SCC Capability Domain is proposed, the consequences (qualification cost and schedule, radiation effects etc.) shall be analyzed and documented. The remaining life time of the selected process shall be confirmed by the foundry. Unless already performed, the feasibility w.r.t. device complexity, packaging, operating frequency and timing shall be assessed.

The foundry shall nominate a technical responsible to be involved during the design work, including attending the design reviews. The foundry shall also formally agree in writing to support the device as a *Standard ASIC* as defined in Appendix B.

The prices for prototype and flight quality components shall be estimated by the foundry, based on the expected manufacturing cost of the devices.

If not previously done, a Development Plan according to section 4.3 shall be established, also including the above information.

Output: Functional Specification (if not previously existing);
Development Plan containing the above information (if not previously existing);
Work Package report (if information not provided in the Development Plan).

2.4 Architectural Design

The architecture of the device shall be defined by partitioning the functions on the block level, clearly specifying the functions, interfaces and interactions of each block. The work shall take into account the subsequent implementation. The corresponding VHDL model shall be developed according to the requirements for VHDL models for component simulation as specified in AD2. However, it is recommended to also be compliant with the requirements for board-level simulation models already at this stage.

A Verification Plan shall be established, defining how the functionality of the design shall be verified.

Unless otherwise specified, there shall be one progress meeting in the middle of the Architectural Design, where the preliminary architecture and the Verification Plan shall be reviewed.

VHDL board-level simulation shall be performed using the developed VHDL model in one or several VHDL testbenches, demonstrating all operating modes and functions of the device, in accordance with the Verification Plan. Surrounding components need only incorporate functions and interfaces (including timing modelling) required to properly simulate the device.

Using the above VHDL testbench(es), a test suite verifying the full functionality shall be developed, and its code coverage verified as specified in AD2. The verification shall follow the established Verification Plan, and shall be performed by somebody other than the designer, to avoid that a mistake in the design is masked by the same mistake in the verification.

The timing of the external interfaces shall be estimated based on the selected process and the design complexity, and the values shall be confirmed by the foundry. It is recommended that the preliminary timing is included in the VHDL model already at this stage. Worst case timing analysis of the external interfaces shall be performed.

The feasibility shall be re-assessed, considering issues such as complexity, packaging, operating frequency, metastability and other possibly critical issues. A full analysis need only to be performed for potentially critical cases.

The production test strategy for the ASIC shall be established. The method to test each block shall be defined, to ensure the realisation of the testability requirements.

A Preliminary Data Sheet of the device shall be established. It shall be comprehensive, containing all parts of the final Data Sheet. Where data is not known, such as for timing, estimates shall be used.

Finally, the results of all work shall be documented in the Architectural Design Document (ADD), and an Architectural Design Review shall be held. Any non-compliancies w.r.t. the requirements and the Functional Specification shall be clearly identified, and are subject to ESA approval.

Output: Verification Plan;
Architectural Design Document according to section 4.5;
Verified VHDL model with test benches according to AD2;
Preliminary Data Sheet according to section 4.8.

2.5 Detailed Design

The gate-level design shall be performed for the selected process and library, fulfilling the requirements of section 3. Only cells approved by the selected foundry should be used; cells not being part of the Capability Approved cell library need prior ESA approval before being introduced.

Production test stimuli and testability circuitry (such as for accelerating counters and for circulating through unused Finite State Machine states after reset) fulfilling the requirements of section 3.2 shall be developed, and the fault coverage verified using fault simulation. In addition, all test stimuli necessary for parameter measurement (electrical tests, timing parameters) shall be developed.

The gate-level design shall be verified against the VHDL model, using the complete test suite from the architectural design; the function shall be proved to be identical on a clock-cycle basis for best and worst case simulations. Any discrepancies need to be approved by ESA. The VHDL model shall then be updated w.r.t. functionality and prelayout timing parameters (if introduced), and the complete test suite re-run.

Radiation effects need only be simulated in case the appropriate tools and libraries are available.

In order to establish the timing margins Static Timing Analysis shall be performed, or alternatively the design shall be simulated at higher operating frequency using appropriate stimuli. Unless otherwise agreed with ESA and the foundry, a margin of 20 % w.r.t. the requirements should be employed for the operating frequency.

The worst case timing analysis of the external interfaces shall be updated with prelayout timing values. The design shall be analyzed with respect to the requirements expressed in section 3.1, which shall be documented in the prelayout Detailed Design Document (DDD). Any non-compliancies w.r.t. the requirements and the Functional Specification shall be clearly identified and agreed with the foundry, and are subject to ESA approval.

The Preliminary Data Sheet shall be transferred to the foundry, and it shall be converted to the foundry's standard format. The contractor shall provide all necessary information and support to the foundry, and shall ensure that the updating can be performed in an efficient way. The foundry shall be responsible for the continued updating of the Data Sheet in this and all following stages.

Previously issued documents shall be updated if necessary. In case there are only minor changes to the ADD, these could instead be included in a separate section of the DDD, subject to prior ESA approval.

Finally, a Detailed Design Review shall be held.

Output: Prelayout Detailed Design Document according to section 4.6;
Updated Architectural Design Document, if necessary;
Updated VHDL model with testbenches;
Updated Preliminary Data Sheet according to section 4.8 (by foundry);
Design database (only upon request).

2.6 ASIC Layout and Final Simulation

The layout shall be performed respecting the ESA/SCC Capability Domain, unless otherwise agreed with ESA. This shall include place and route and test vector conversion if necessary. Special attention should be paid to the clock tree generation and the resulting clock skew, especially for sensitive structures such as shift registers. Layout-driven clock tree generation and placement is recommended. Verification shall include Design Rule Check (DRC), Electrical Rule Check (ERC) and Layout Versus Schematic (LVS) (or Netlist Comparison Check, NCC).

Postlayout simulations shall be performed using the complete previously developed test suite to verify the proper operation; it is not sufficient to only simulate the production test stimuli. In case the design has been modified during the layout, e.g. the clock tree has been rebuilt, the simulations shall be performed on the modified design. The function shall be proved to be identical on a clock-cycle basis for best and worst case simulations for the complete test suite.

The postlayout timing margins shall be established in the same way as in the Detailed Design Work Package. Unless otherwise agreed, a margin of 10 % w.r.t. the requirements should be employed for the operating frequency. The clock tree and its skew shall be analyzed, and shall be approved by the foundry.

The work on the draft ESA/SCC Detail Specification according to AD5 shall be started by the foundry (to be finalised in the *Prototype Manufacture and Test* stage).

Finally, the results shall be introduced in the DDD, and a Postlayout Design Review shall be held. After successful completion and foundry acceptance of the design, the design shall be released for prototype manufacture according to AD1.

Output: Postlayout Detail Design Document according to section 4.7;
Statement of Compliance according to AD1 (by foundry);
Back-annotated postlayout design database (only upon request).

2.7 Prototype Manufacture and Test; Data Sheet and VHDL Model Update

The device shall be manufactured, packaged and tested. The package shall be the same as for flight devices, unless otherwise agreed with ESA. The work shall encompass the full industrialisation of the device, including test program conversion. All necessary hardware such as probe cards, burn-in boards etc. shall be procured in advance.

The manufactured devices shall be tested against the draft ESA/SCC Detail Specification, at least covering full table 2 measurements. Unless otherwise agreed, the functional tests shall be performed at the rated operating frequency of the device. Timing tests shall include setup and hold times on all inputs, and output delays on all outputs. The tests need only be performed at room temperature. Timing values specified as an integer number of clock cycles need only be verified by the functional tests.

The Data Sheet shall be updated with correct figures for electrical, timing and power consumption parameters. The draft ESA/SCC Detail Specification shall be completed and submitted to ESA/SCC Secretariat as per AD5. Values measured after the manufacture shall be used in both cases.

If not previously done, the VHDL model shall be updated to a model for board-level simulation according to the requirements of AD2, using timing parameters obtained after the manufacture.

Output: Packaged tested devices;
Production Test Report according to AD1;
Data Sheet according to section 4.8 (by foundry);
Draft ESA/SCC Detail Specification according to AD5 (by foundry);
VHDL model for board-level simulation and its testbenches according to AD2;
VHDL model User's Manual according to AD2.

2.8 Transfer of Design and Knowledge; Support Commitment

In addition to the complete design documentation and the database, sufficient knowledge about the design shall be transferred free of charge to the foundry, enabling it to give support to a level corresponding to a *Standard ASIC*. The foundry shall free of charge be given a license allowing unlimited rights to modify, manufacture and market the device and any derivative thereof. The foundry shall analyze the delivered design database, and confirm its completeness in writing.

The foundry shall provide a formal written commitment to market the ASIC, to make it available to European Industry on equal conditions, to preserve the design database and the ASIC mask data for minimum ten years, and to provide basic application support to board designers at a level corresponding to a *Standard ASIC* as defined in Appendix B. Furthermore, the foundry shall establish the price of the device in prototype and flight quality levels as specified in Appendix B. The foundry shall confirm the remaining life time of the process used.

An Experience Summary Report shall be written jointly by the designer and the foundry.

If a Final Presentation is to be held, it should be focused on the device and its intended usage on-board spacecraft in order to promote it for ESA projects.

Output: Confirmation of database completeness;
Commitment to provide the device as a *Standard ASIC*, including pricing;
Experience Summary Report according to AD1.

2.9 Design Validation (Waived by default)

This stage need only be performed if explicitly requested.

A Validation Plan shall be established, where possible reusing parts of the Verification Plan. In case the device was manufactured outside the ESA/SCC Capability Domain or used specially developed cells, the validation tests shall include complete radiation testing (total dose, Single Event Upset and Latch-up), unless proved not to be necessary.

The manufactured devices shall be validated according to the Validation Plan, by designing and building a breadboard representative of a realistic application and performing validation tests covering the full functionality and all operating modes of the device. The results shall be documented in a Validation Test Report.

The Data Sheet shall be updated based on the experience gained from designing the breadboard, the validation, and other possible sources.

Output: Validation Plan;
Validation Test Report according to AD1;
Updated Data Sheet according to section 4.8.

2.10 ESA/SCC Qualification (Waived by default)

This stage need only be performed if explicitly requested. However, it should be considered for devices developed within the ESA/SCC Capability Domain, since the qualification is rather simple in such cases, and in the view that a qualified device is more attractive to use for a company or project.

Output: Devices placed on the Qualified Part List (QPL);
Finalized ESA/SCC Detail Specification.

3 SPECIFIC REQUIREMENTS

3.1 Design Requirements

The design work shall be structured to produce designs of high quality being suitable for space applications. As a minimum the requirements of the following subsections shall be fulfilled.

3.1.1 Reset

The design shall be fully deterministic, and it shall be in a fully known state after reset. Using synchronous reset instead of asynchronous requires a justification, since it could cause simulation problems when logic synthesis has been used, and also might decrease the fault coverage.

It is suggested that the reset signal is a Schmitt trigger input with synchronisation.

3.1.2 Synchronous Design

Wherever possible the design shall be synchronous according to the following definition:
- The number of clock regions shall be minimised;
- Every latch and flip-flop within a clock region shall be connected to the same clock source with only buffers inserted for the purpose of increasing the driving strength or using another clock edge (no logic functions or memory elements are allowed);
- The clock tree for each clock region should be optimally balanced;
- In case clock tree branches with shorter or longer delays are used (e.g. for decreasing the clock-to-output delay) the impact shall be analyzed;
- Control and data signals between different clock regions shall be synchronised;
- The device function shall not be dependent on internal signal delays.

3.1.3 Metastability

The possibility of metastability phenomena shall be reduced; the Mean Time Between Failure (MTBF) caused by metastability shall be minimum 100 years in total for one device. The impact of metastability failures shall be assessed and documented.

3.1.4 Low Power Consumption

The device shall be designed for low power consumption, e.g. using static logic, using divided clocks and stopping clocks where appropriate (including performing a trade-off versus using a fully synchronous design).

3.1.5 Power Supply Connections

The number of power supply connections shall be sufficient to guarantee the proper operation of the device in all foreseen applications.

3.1.6 Single Failures and Single Event Upsets

The consequences of single failures and Single Event Upsets (SEUs) leading to the device entering a non-recoverable state shall be minimised. Typical examples include that all unused states of a Finite State Machine shall lead to a used state (e.g. the reset state) and that it must be possible to reload configuration registers in case an SEU has changed the operating mode of the device.

3.1.7 Floating Nodes

It shall be ensured that tristate signals are always driven except for a short period (typically 0.5 to 2 clock cycles) when switching between drivers, internally on the device as well as for external signals and busses (eliminating the need for external pull-up or pull-down resistors).

3.1.8 Bus Contention

It shall be ensured that bus contention (collision) cannot occur, internally as well as externally. Specific attention shall be paid to the behaviour at reset, especially in case the reset signal is internally synchronised since bus contention could occur between reset is asserted and the active clock edge occurs.

3.1.9 Glitch-free Outputs

It shall be ensured that no output will produce glitches during normal operation.

3.1.10 Unsuitable and Unnecessary Circuitry

Library elements and circuitry unsuitable for the intended environment shall not be used unless necessary. Dynamic logic shall not be used.

The design shall not incorporate more circuitry than necessary. In particular, redundant and unused circuitry should be removed where possible since it decreases the testability and device reliability.

No cell inputs shall be connected to the power supply rails, except where necessary for the functionality.

3.2 Testability

The concept for fault coverage calculation is based on RD1, with some simplifications and heuristic methods introduced for practical reasons. However, the contractor may propose to calculate the fault coverage in full compliance with RD1, subject to ESA agreement (all other testability requirements shall remain as specified in this document).

3.2.1 Testability Requirements

For testability purposes the design can be considered as consisting of two different categories of logic:

- *Gate Logic* consists of logic primitives such as inverters, AND gates, flip-flops etc. This normally includes structured logic built of such logic primitives, e.g. multipliers, adders etc., unless where a particular structure clearly belongs to the *Block Logic* category;
- *Block Logic* is complex regular components such as Random Access Memories (RAMs), Read Only Memories (ROMs) and Programmable Logic Arrays (PLAs).

The testability requirements for the production test shall include:

- The base fault coverage for *Gate Logic* shall be minimum 95.0 % (98.0 % if explicitly required);
- For RAMs, established march tests shall be used, with a minimum requirement of 100 % stuck-at fault coverage, preferably also covering stuck-open and bridging faults;
- For ROMs, it shall be proved that all significant data on all addresses have been accessed and propagated to the outputs;
- For other *Block Logic* types the testability approach shall be agreed with ESA before commencing the development, where possible using established testing algorithms.

For *Gate Logic* the ratio of faulty devices passing production test is generally higher when using internal scan compared when using non-scan based production test at the same level of fault coverage. Therefore internal scan shall be combined with non-scan based production test. The combined fault coverage for the scan based and non-scan based production tests together shall be higher than the specified base fault coverage, according to the following formula:

Combined fault coverage = base fault coverage + 0.2 • (base fault coverage - non-scan fault coverage)

The combined fault coverage as a function of the obtained non-scan fault coverage is shown below, for a base fault coverage of 95 % and 98 %, respectively.

Base fault coverage	Non-scan fault coverage 80 %	Non-scan fault coverage 90 %	Non-scan fault coverage 95 %	Non-scan fault coverage 98 %
95.0 %	98.0 %	96.0 %	95.0 %	95.0 %
98.0 %	-	99.6 %	98.6 %	98.0 %

In addition, for *Gate Logic* 100 % node toggle test shall be performed. A list of nodes not toggled shall be provided, as well as a list of all faults not detected by the fault simulation.

As a baseline, the number of test vectors shall be less than 64000, and otherwise the capability of the ASIC tester to be used shall be assessed.

In case of special testing methods being applied, such as Crosscheck technology or I_{DDQ}-based testing, the testability requirements should be agreed with ESA before commencing the development.

If specified, Built-In Self Test (BIST) shall be implemented to obtain the specified fault coverage within the maximum time period allowed. It shall be possible to disable the BIST function. The consequences of errors in the BIST circuitry shall be assessed and documented. If not otherwise specified, the result of the BIST should be reported using an ERROR pin, which shall be in the error state while the BIST is performed (suggested value: '0' since an un-powered device will then indicate error). The BIST result shall not depend on the state of the input pins, and all output pins shall be inactive while the BIST is performed.

The IEEE 1149.1 Boundary Scan (JTAG) interface may be proposed by the contractor subject to ESA agreement. The contractor shall then indicate how this interface will be used referring to at least one actual case (the general case of using Boundary Scan is known and need not be explained).

3.2.2 Calculation of Fault Coverage

As a baseline, the fault coverage shall be related to the stuck-at fault model at the gate-level, faulting all inputs and outputs (called *logic lines* in RD1) of each gate. However, if this is not supported by the library or fault simulator, the fault coverage may be calculated only related to the outputs of each gate, with a penalty factor for the fault coverage according to:

Outputs-only fault coverage = 50 % + (Inputs&Outputs fault coverage)/2

The faults may be reported as non-collapsed or collapsed, as supported by the fault simulator used.

Only hard detects shall be accounted for, possible faults may only be counted if it can be shown that they actually will be detected, not involving an X value. However, in reality some of the possible faults will be detected by resetting the device followed by continued testing. Repeating this procedure with the device in a different internal state will detect some additional faults. Therefore, under the conditions specified on the next page, it is allowed to count a fraction of the possible faults as detected, up to maximum 5 % of the total number of faults, according to:

Faults counted as detected = (Possible faults) • (1 - 1/N)

N represents the number of times the device has been reset after the initial reset, under the following conditions:

- To obtain a reasonable difference in the internal state before each reset, the device shall be clocked for minimum 500•*i* clock cycles before the *i*:th reset, i.e. as a minimum the device shall be clocked for 500 clock cycles before the first reset, 1000 clock cycles before the second, 1500 clock cycles before the third reset, etc.;
- To allow the faults to be propagated to the primary outputs for detection, the test must continue for minimum 500 test vectors after a reset.

Tristate faults may only be accounted for if it can be shown that they will be detected by the actual Automatic Test Equipment (ATE) to be used.

Faults that can be considered as undetectable are unconnected outputs of gates, inputs connected to constant logic values and faults resulting from deliberately designed logical redundancies. In addition, possible faults originating from the enable signal of internal tristate buffers may be regarded as undetectable.

For the fault simulation, test stimuli shall be applied to the primary inputs of the device in exactly the same way it will be applied by the ATE, and faults shall only be detected using the primary outputs of the device, as they would be detected by the ATE. All limitations of the ATE including any fully or partially masked test vectors shall be taken into account for the fault coverage calculation.

Built-In Self Test (BIST) implementations commonly use a Linear Feedback Shift Register (LFSR) or similar for compacting the output responses from a logic block. At the end of the test, (part of) the LFSR content is compared with a known value to determine whether an error was detected. Frequently a node of the LFSR is observed during fault simulation to reduce the simulation time. However, fault coverage reduction caused by aliasing in the LFSR is then not handled. Therefore, in case an internal node of an LFSR is observed for a sub-test, a penalty value shall be applied to the resulting fault coverage of each such sub-test according to:

Reported sub-test fault coverage = (1 - p) • Measured sub-test fault coverage

The penalty value *p* depends on the degree *k* as defined below. The degree *k* shall be the lowest the LFSR degree and the number of LFSR bits used by the BIST circuitry for determination of the BIST outcome (e.g. if only one bit from the LFSR is used for the detection *k* is 1).

Degree *k*	$k < 8$	$8 \leq k < 16$	$16 \leq k < 24$	$k \geq 24$
Penalty *p*	1.00	0.05	0.01	0.00

4 DESIGN DOCUMENTATION

All documentation shall be in English. The documentation shall be well structured and easily readable, so that the design can be understood by an ASIC designer not being involved in the design work. Names of signals, blocks etc. shall be chosen to indicate their function, and shall be based on English. The documentation shall be consistent, e.g. the same item shall have the same name in all documentation.

Block diagrams, control flow charts, timing diagrams and other figures shall be introduced where beneficial for the understanding of the text.

Every time an updated document is delivered it shall include a detailed change list, and all significant changes marked using a change bar in the margin. If a document is delivered before being complete, each page with incomplete information shall be clearly marked.

Some of the information listed is normally better delivered separately or in appendices, such as layout plots, gate-level schematics, lists of undetected faults etc.

4.1 ASIC Requirement Specification

The purpose of the ASIC Requirement Specification shall be to provide all information necessary to allow an assessment of whether the device will accomplish its intended function. All information necessary for the subsequent work with the Functional Specification shall be included, using a structured and logical organisation.

High-level requirements shall be precisely expressed, whereas low-level requirements could sometimes be expressed by reference to interfacing devices. As an example, requirements of an interface to an external RAM could be expressed by specifying the memory size or bus widths, whereas the timing requirements and the control signals could be expressed as a requirement to be compatible with certain, identified RAMs.

A presentation of all foreseen system configurations using the device shall be included, identifying external devices and protocols to be interfaced, as well as the system partitioning, e.g. on several board or units. Other issues to be dealt with include applicable algorithms, system testing, power dissipation, operating environment and reliability. The reason for each requirement should be explained.

Thereafter all requirements on the device itself shall be specified, including but not limited to:

- Functionality, operating modes, initialization, state after reset and error handling;
- Functionality for system test, e.g. in-flight and ground tests;
- Programmability as required by associated software;
- Interfaces and signals;
- Target performance, including operating frequency, power dissipation, timing of critical signals, etc.;
- Operating conditions, including temperature, supply voltage, radiation etc.

4.2 Feasibility Report

The purpose of the Feasibility Report shall be to allow the feasibility of the development to be judged. The report shall include but not be limited to:

- Availability and quality levels of the potential process technologies;
- Possibility that the requirements can be met by the potential process technologies and whether the design will reach any technical limitations such as complexity, operating frequency and packaging limitations such as the number of pins.

The risk analysis shall identify critical issues and possible backup solutions, including but not limited to:

- Maturity of foreseen manufacturers, including tools and design libraries supported;
- Availability of engineering resources and their experience and familiarity with the design type, tools, technology and the potential foundries;
- Stability of the requirements and possibility of requirement changes.

4.3 Development Plan

The purpose of the Development Plan shall be to allow an assessment of the proposed development strategy. It shall include issues applicable to the work to be done in the activity. Non-applicable information, such as tools available but not intended to be used in the activity, shall not be included. The development plan shall include, but not be limited to:

- Design flow, e.g. for design capture, logic synthesis, back annotation etc.;
- Design analysis and verification approach;
- Identification of the baseline process and library. The suitability for the application and the status regarding ESA/SCC Capability Approval shall be assessed;
- Identification of the baseline package and is suitability for space application;
- Identification of all design tools to be used, including their version and platforms. The availability of each tool (at the site as well as the dedication to the particular development) shall be explicitly stated. The status and availability of the ASIC libraries for each of the tools to be used shall be assessed;
- Identification of companies involved, and their specific tasks and interaction;
- Specification of in which formats design data, test vectors etc. will be transferred from the designer to the foundry, and from the foundry back to the designer (e.g. if back annotation to the designer will be performed). In case the *Architectural* and *Detailed Design* stages are split between different contractors, the exact split and responsibilities shall be specified in detail, together with the relevant formats for transferring the design data, test stimuli etc.;
- Testability and test vector generation approach, including test coverage verification approach and an estimate of the number of test vectors;
- Identification of limitations on the equipment to be used for production test, including the tester memory depth and the testing frequency;
- Detailed description of how the knowledge shall be transferred to the ASIC manufacturer, to enable them to support the device as a *Standard ASIC*;
- Validation approach (if included in the development);
- Qualification approach (if included in the development);
- List of deliverable items and their format.

4.4 Functional Specification

The purpose of the Functional Specification shall be to fully and clearly specify the device to be designed, fulfilling all requirements of the ASIC Requirement Specification. In case a requirement cannot be fulfilled, the discrepancies shall be fully documented.

The Functional Specification shall be self-contained and there shall be no need to consult other documents in order to understand what shall be implemented, except when external interfaces are specified to be compliant with certain identified components. It should be structured to easily be transformed into a Data Sheet as per section 4.8.

Trade-off discussions shall be avoided in the Functional Specification, except when background descriptions are necessary for the overall understanding of the functionality. Issues unnecessary reducing the design space available for the *Architectural Design* should be avoided, e.g. overly specifying interfaces under the full control of the device.

All functions and requirements shall be specified in a clear and precise manner, including but not limited to:

- Description of all foreseen system configurations in which the device can be used, including external devices and interface protocols (from the ASIC Requirement Specification);
- Bit numbering and naming convention (to be maintained throughout the design flow);
- Format of data structures;
- Functionality, including operational modes and requirements for system test;
- Protocols and algorithms used;
- Error handling;
- Definitions of programmable registers and their initialization;
- State after reset for signals and internal registers;
- Identification of functions not included in the device, to avoid potential misunderstandings;
- High-level block diagram indicating data and control flows;
- Specification of all interfaces and signals, including power supply and test pins;
- Operating conditions;
- Specification of all electrical parameters;
- All target timing parameters (setup and hold times, output delays etc.) with corresponding waveform diagrams;
- Baseline package.

4.5 Architectural Design Document

The purpose of the Architectural Design Document (ADD) shall be to allow the proposed architecture to be analyzed. All results shall be documented to such level that the *Detailed Design* can commence using only the Functional Specification and the ADD as the specification of the design.

There shall be a clear correspondence between the Functional Specification and the ADD. Information already included in the Functional Specification need not be duplicated in the ADD.

An introduction to the architecture shall be given, including:
- Block partitioning and its rationale;
- Internal protocols and data formats;
- Interfaces and protocols to external devices, including memory mapping;
- High-level block diagram including data and control flows;
- Overview of the corresponding VHDL model.

Thereafter the architecture shall be described in detail, including:
- Block diagram corresponding to the actual decomposition of the design and all signals, together with a description of the block interaction;
- Test architecture and interfaces, described separately or for each block, including reset generation and Built-in Self Test where applicable;
- Full description of each block, including:
  - Purpose and overview of functionality;
  - Interfaces to the block and associated requirements;
  - Structure of the block and description of sub-blocks, if applicable;
  - Detailed functionality, including description of finite state machines using graphs, type of state machine encoding and handling of unused states;
  - Testability circuitry for the block.

If custom cells need to be developed, complete specifications shall be included.

The results from the feasibility analysis of the architecture shall at least include:
- Preliminary worst case timing analysis of external interfaces;
- Complexity, packaging, operating frequency, power dissipation and metastability.

The verification of the architecture shall be documented, including textual descriptions of the verifications performed and results obtained, descriptions of all stimuli and testbenches, and the VHDL code coverage results. A compliance matrix shall be included confirming the correspondence between the ADD and the Functional Specification.

If the ADD has been updated after the *Detailed Design*, this shall be clearly indicated on the front page.

4.6 Prelayout Detailed Design Document

The purpose of the prelayout Detailed Design Document (DDD) shall be to document that all requirements on functionality, testability and design methodology have been met, including documentation of simulation and analysis results.

All information necessary for the subsequent work, such as layout and manufacture, shall be clearly expressed. In addition, all information necessary to allow a possible future redesign or retargeting to another process should be included, to an extent allowing it to be performed by another designer.

The prelayout Detailed Design Document shall be updated after the *ASIC Layout and Final Simulation* stage as described in section 4.7.

To avoid potential errors, information from already established documents can be referenced using a complete reference (document title, reference number, issue number and date, section). However, in case information is only partly correct, it is better to include a fully correct version.

Where possible, the block decomposition from the *Architectural Design* should be maintained.

All information necessary to implement each block as well as circuitry introduced during the *Detailed Design* stage shall be shall be documented, including:
- Further decomposition of the blocks into sub-blocks or gates when applicable;
- Test circuitry and its operation;
- Synthesis constraints for each block and block grouping;
- Identification of ASIC library buffers used for the interfaces;
- Layout constraints for the distribution of clock, reset, power and critical nets;
- Floor plan;
- Description of cells specially developed for the design;
- Hierarchical gate-level schematics.

The gate-level schematics shall be coherent with the block diagram. They shall be easily readable, e.g. inputs shall be to the left, outputs to the right. Invisible information, such as global nets, shall be avoided. The schematics shall represent the complete structural information down to the ASIC library cell/gate level. Automatically generated schematics are only accepted for modules synthesized from behavioral non-structural VHDL code, provided that they are reasonably readable. Schematics with connections by netname will not be accepted.

The gate-level simulations shall be documented, including a textual description of the stimuli and expected responses. Analysis results of error and warning messages from the simulations shall be documented. The comparisons between the VHDL and the gate-level simulation results shall be documented. A summary of the gate-level simulation results shall be included and a verification matrix shall be established. If the VHDL model has been modified, the results of test suite re-run shall be included.

The production test program shall be documented, including a textual description of the test vector generation methods, power measurement and parametric tests.

The fault simulation results shall be documented for the production test, and if applicable for the BIST. The results for each sub-test shall be presented, including the fault categories (detected, undetected faults, possible and tristate faults) and the number of test vectors. The fault coverage calculation shall be documented including faults declared as undetectable and primary outputs used for each sub-test, and a summary of the results shall be provided. A list of undetected faults shall be provided.

The toggle test shall be documented, and a list of nodes not toggled shall be provided.

The analysis performed shall be documented, including but not restricted to:
- Worst case analysis timing analysis of interfaces, using prelayout timing values;
- Timing margins established using static timing analysis or other methods;
- Clock tree and clock skew analysis;
- Fan-out and wire load analysis;
- Package specification and preliminary pin assignment;
- Gate count, die size and analysis w.r.t. the package cavity size;
- Results from foundry specific rule checkers, if any;
- Analysis of design requirements as per section 3.1. Each requirement shall have a separate section in the DDD, it is not sufficient to only state full compliance.

The organization of the complete design database shall be fully described, including the file structure, naming conventions and version control. All tools and ASIC libraries actually used during the *Detailed Design* shall be documented.

A compliance matrix shall be included showing the correspondence between the DDD and the Functional Specification, and a summary of any discrepancies shall be provided.

4.7 Postlayout Detailed Design Document

The purpose of the Postlayout Detailed Design Document shall be to document the information resulting from the *ASIC Layout and Final Simulation*. Issues previously not documented or updated information shall be documented, including:
- Postlayout clock distribution tree and clock skew analysis;
- Layout plot, bonding diagram and final die size;
- Postlayout verification and analysis of timing margins;
- Results from the Design Rule Check (DRC), Electrical Rule Check (ERC) and Layout Versus Schematic (LVS) (or Netlist Comparison Check, NCC).

All preliminary results or estimates in the Prelayout DDD shall be updated with values obtained during the *ASIC Layout and Final Simulation*.

The compliance matrix w.r.t. the Functional Specification shall be updated.

The front page shall clearly indicate that the document has been updated after the *ASIC Layout and Final Simulation*.

4.8 Data Sheet

The purpose of the Data Sheet shall be to describe the functionality of the device so it can be used by a board or system designer. The text shall be oriented towards the user, and irrelevant information should not be included. Particular information useful for space applications shall be included. A Data Sheet for a commercial device can be taken as an example of the level of detail and presentation style. An example Data Sheet can be provided by ESA upon request.

Each page shall contain the foundry name, the device name and number and the date of issue. It is recommended that the first page contains a summary of the device functionality, a block diagram and short list of features, such as operating frequency, technology etc., and the foundry address.

All characteristics and limitations introduced during the design shall be described, such as detailed interface descriptions, register definitions, memory maps etc.

The Data Sheet shall include a system overview of the device and a description of how to use the device in a typical system, including an application block diagram.

The full functionality and all operating modes shall be specified in detail, as per the last paragraph of section 4.4 (Functional Specification).

All signal interfaces shall be described in detail including description of all signals, test and power pins etc., specifying the usage of the signals, the signal polarity etc. The signal descriptions shall be grouped according to their function.

All electrical and mechanical data shall be specified, together with their relevant applicable conditions (temperature, capacitive load etc.), including:

- Absolute maximum ratings, including storage temperature, operating temperature, supply voltage, maximum input current for any pin, total dose, Single Event Upset, latch-up, electrostatic discharge and reliability figures;
- DC parameters, including voltage levels, leakage currents, pin capacitances and output currents;
- Static and dynamic (per MHz) power dissipation, allowing the power consumption at lower operating frequencies to be calculated;
- AC parameters, including setup and hold times, cycle periods, output delays, tristate delays etc., together with waveform diagrams. The timing parameters shall be related to the relevant reference signal edges;
- Package description, including pin assignment, package figure with pin numbers and preferably signal names, and a mechanical drawing for the package dimensions.

One Application Note for a sample design, including component level schematics, shall be provided in the same format as the Data Sheet. Where possible, European components shall be used in this application note.

A Preliminary Data Sheet shall contain all parts of a final Data Sheet, with the same level of detail. Where data is not known, estimates shall be used.

5 DELIVERABLE ITEMS

Design review packages	3 paper copies
Functional Specification, if applicable	5 paper + 1 electronic copy
Preliminary Data Sheet (during development)	3 paper copies (1 unbound)
Final Data Sheet	20 paper + 1 electronic copy
Draft ESA/SCC specification	1 paper copy
Production Test Report	2 paper copies
Draft documents	3 paper copies
Other reports and documents	3 paper + 1 electronic copy
All VHDL code, including all related files as specified in AD2	1 paper + 1 electronic copy
VHDL model User's Manual	10 paper + 1 electronic copy
All schematics	1 paper + 1 electronic copy
Complete ASIC design database, including verification & test stimuli and results, schematics, synthesis scripts etc. All information needed to reproduce and/or redesign the device shall be included.	1 electronic copy
EDIF gate-level netlist of final design, including changes introduced during layout	1 electronic copy
Test vectors in a format suitable for the foundry	1 electronic copy
Colour plot of the layout	2 paper copies, min. 1 x 1 m
Colour photograph of manufactured die	1 35 mm slide positive + 1 A4 view-graph positive
Packaged tested device prototypes	20

Upon request, ESA shall receive free of charge, for the duration of the development, a complete design kit for the selected process, including all libraries and design kit tools and their complete documentation, in order to allow ESA to independently verify the design. This only applies if such a design kit actually exists for the design tools available at ESTEC.

Each delivery of a design document, VHDL model or design database shall be accompanied by a written statement clearly identifying to what extent the deliverable item has been reviewed w.r.t. the applicable requirements, notifying any discrepancies, whether previously agreed or not. This shall include the level of verification performed if the delivery occurs before the verification has been completed, including the VHDL model code coverage when applicable.

Paper copies shall be easily readable and suitable for subsequent photo-copying. Electronic copies shall be submitted on a media and in a format as agreed with the ESA technical officer, the baseline being properly marked QIC-150 tape cartridges suitable for archive storage, restorable on a Sun Sparc workstation using the Unix *tar* command.

Text files shall be in WordPerfect, FrameMaker or ASCII format (for documents ASCII only after ESA agreement).

Photos and layout plots shall be properly marked to be suitable for official presentation. They shall be supplied with a written statement permitting ESA to use them in ESA publications and exhibitions free of charge.

ESA shall have the right of access to the VHDL models developed (including testbenches and necessary packages) in accordance with the contract conditions.

The design database delivered to ESA will only be used within ESTEC. Nevertheless, when the device will not anymore be available nor supported as a *Standard ASIC*, ESA reserves the right to make the design database available to any ESA contractor or project free of charge. The same applies to any design derived from the one developed.

Acceptance of deliverable items

Provisional acceptance will be given upon reception and brief review of each deliverable item. Final acceptance will be given within three month of the reception of all deliverable items, if no discrepancies are found between the specifications - including agreed changes - and the delivered items.

If a design is delivered without subsequent manufacturing, it will be accepted upon approval of the design database and documentation.

APPENDIX A: ABBREVIATIONS

ADD	Architectural Design Document
ADID	ASIC Design Initiation Document
ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
ASSP	Application Specific Special Product
ATE	Automatic Test Equipment
BIST	Built-In Self Test
CAD	Computer Aided Design
DDD	Detailed Design Document
DRC	Design Rule Check
EDIF	Electronic Design Interchange Format
ERC	Electrical Rule Check
ESA	European Space Agency
ESTEC	European Space Research and Technology Centre
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IEEE	Institute of Electrical and Electronics Engineers
JTAG	Joint Test Action Group, the IEEE 1049.1 boundary scan test method
LFSR	Linear Feedback Shift Register
LVS	Layout Versus Schematic
MTBF	Mean Time Between Failure
NCC	Netlist Comparison Check
PLA	Programmable Logic Array
QIC	Quarter Inch Cartridge
QPL	Qualified Part List
RAM	Random Access Memory
ROM	Read Only Memory
SEU	Single Event Upset
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

APPENDIX B: DEFINITION OF *STANDARD ASIC*

A *Standard ASIC* (sometimes referred to as an *Application Specific Standard Product*, ASSP) is defined as a device developed in the same way as an ASIC, but with the intention to be widely used by other companies, in a way similar to a standard component. It has the following characteristics:

- The device is normally designed in the same way as an ASIC, normally by another company than the foundry;
- The device is manufactured as an ASIC;
- After the development, the device shall be available to European companies under equal conditions from the foundry, including distributing data sheets and basic support to potential customers.

To allow the device to be efficiently used, basic application support to board designers is necessary. Supporting a device as an *Standard ASIC* shall include:

- Distributing the Data Sheet and related documents to all potential customers;
- Distributing the VHDL model for board-level simulation to all potential customers (this VHDL model need not be synthesizable and may be encrypted in order to protect the design);
- Providing information about the device functional behaviour and characteristics to users, to the extent possible given by the involvement during the design work and the design database;
- Updating of the Data Sheet in case incorrect, misleading or missing information is identified.

It is acceptable that support at the system level (i.e. how to design a subsystem using the device) is limited to distributing such information when available, and the foundry is not required to obtain full system-level knowledge.

In case there is a price associated with the Data Sheet or the VHDL model to be used in an ESA activity, this shall only cover the distribution, maintenance and support costs for the respective items.

Each device shall be available as a minimum in prototype and flight quality levels, with prices based on the production costs of the device. The prices should be comparable to other devices of similar complexity.

To ensure the long term availability of the devices, the complete design database and the ASIC mask data must be preserved for minimum ten years by the foundry.

APPENDIX C: DOCUMENTATION OUTLINES

This appendix contains suggested outlines of some documents, as a guide for the contractor. However, it should be noted that they are not necessarily complete. In case of discrepancies, the requirements have precedence over these outlines.

Certain items could be included as appendices or separately when this would increase the readability, such as layout plots, schematics, scripts etc.

C.1 Development Plan

Introduction
- Applicable and reference documents
- Acronyms and abbreviations

Development Plan
- Design flow
- Design analysis and verification approach
- Baseline process and library
- Baseline package
- Design tools, versions and platforms
  - VHDL simulator(s)
  - Schematic entry tools
  - Logic synthesis tools
  - Prelayout gate-level simulation tools
  - Postlayout gate-level simulation tools
  - Fault simulation tools
  - Static timing analysis tools
  - Netlist generation tools
  - Test vector generation tools
  - Availability of tools
- Libraries and ASIC design kit
  - ASIC libraries *{For each tool intended to be used}*
  - ASIC design kit and associated manuals
  - Library status
- Companies involved
- Design data formats
- Testability and test vector generation approach
- Test coverage and verification approach
- Production test equipment and limitations
- Transfer of design knowledge
- Validation approach
- Qualification approach
- Deliverable items and formats

C.2 Functional Specification

Introduction
- Applicable and reference documents
- Acronyms and abbreviations
- Discrepancies w.r.t. the ASIC Requirement Specification

Functional description
- Summary of operation
- Functions not included
- Numbering and naming conventions
- Data formats
- Block diagram
- Description of all foreseen systems using the device
- Functional specification
  - *{Description of all functions}*
  - Operational modes
  - Protocols and algorithms
  - Initialization
  - Programmable registers
  - Error handling
  - Functionality for system test
  - State after reset

Interfaces and signal description
- Signal description *{Grouped after function}*
- Preliminary test, power and ground pins

Electrical and mechanical specification
- Absolute maximum ratings
  - Operating temperature
  - Supply voltage
  - Electrostatic discharge
  - Radiation environment
  - Reliability
- DC parameters
  - Input and output voltages
  - Input leakage currents
  - Input and output capacitance
  - Static and dynamic power dissipation
- AC parameters
  - Operating frequency
  - Timing parameters and waveforms
- Mechanical data
  - Package specification

C.3 Architectural Design Document

- Introduction
  - Applicable and reference documents
  - Acronyms and abbreviations
  - Numbering and naming conventions
  - Discrepancies w.r.t. the Functional Specification
- Architectural description
  - Block partitioning
  - Data formats and protocols
  - High-level block diagram with data and control flows
  - External devices and protocols
  - VHDL model overview
  - Detailed architecture description
    - Block diagram
    - Block interaction
    - Test architecture and interfaces
      - Reset generation
      - Built-in Self Test
    - Block descriptions *{For each block}*
      - Purpose and overview of functionality
      - Interfaces
      - Internal structure
      - Detailed functionality
        - State machine graphs and encoding
        - Handling of unused states
      - Test circuitry
- Custom designed cell specifications
- Feasibility analysis of the architecture
  - Preliminary worst case timing on external interface
  - Operating frequency
  - Power dissipation
  - Metastability
  - Complexity and packaging issues
- Architectural verification results
  - Description of simulations performed and results obtained
  - Test stimuli description
  - VHDL code coverage
- Compliance matrix w.r.t. the Functional Specification

C.4 Detailed Design Document

Introduction
- Applicable and reference documents
- Acronyms and abbreviations
- Numbering and naming conventions
- Summary of discrepancies w.r.t. the Functional Specification
- Architectural modifications w.r.t. the ADD

Detailed design description
- ASIC I/O buffers
- Layout constraints
- Block descriptions *{For each block}*
  - Synthesis constraints *{Scripts as appendix}*
  - Test circuitry description
- Schematics and netlists *{As appendix}*
- Floor plan

Custom cell description

Gate-level simulation
- Gate-level simulation description and results
- Comparison between the VHDL and the gate-level simulations
- Error messages and warnings during simulations
- Verification matrix
- Summary of results

Production test
- Test program description
- Test vector generation
- Parametric tests
- Power measurement

Fault simulation
- Fault simulation results
- Fault coverage calculation
- Toggle test result
- List of undetected faults and not toggled nodes *{As appendix}*
- Summary of results

Detailed analysis
- Worst case timing of interfaces
- Static timing analysis and clock skew
- Fan-out and wire load
- Package specification
- Die size
- Foundry rule checker results
- Reset circuitry
- Synchronous design
- Power consumption
- Power supply connections
- Metastability
- Single Failures and Single Event Upset
- Floating nodes
- Bus contention

Glitch-free outputs
Unsuitable and unnecessary circuitry
Postlayout results
Design Rule Check (DRC)
Electrical Rule Check (ERC)
Layout Versus Schematic (LVS)
Netlist Comparison Check (NCC)
Chip statistics
Bonding diagram
Layout plot *{Separately}*
Design database organization
Design tools and ASIC library configuration
CAD tools used
ASIC foundry's tools and libraries used
Compliance matrix w.r.t. the Functional Specification

C.5 Data sheet

{Header}
Foundry
Technology
Device name and number
Date

{Front page}
Description
Block diagram
Features
Foundry address

Table of contents
Introduction
Reference documents
System overview
Description of a typical system using the device
Block diagram of a typical system

- Functional description
  - General description
    - Summary of operation
  - Functions not included
  - Functional specification
    - *{Description of all functions}*
    - Operational modes
    - Initialization
    - Registers
    - Programming
    - Memory mapping
    - Error handling
    - Test functions
    - State after reset
- Interfaces and signal description
  - Signal overview figure
  - Signal description *{Grouped after function}*
  - Test pins
  - Non-connected pins
  - Power and ground pins
- Electrical and mechanical data
  - Absolute maximum ratings
    - Storage temperature
    - Operating temperature
    - Supply voltage
    - Maximum input current any pin
    - Total dose
    - Single Event Upset
    - Latch-up
    - Electrostatic discharge
    - Reliability
  - DC parameters
    - Input and output voltages
    - Input leakage currents
    - Output currents
    - Capacitances
    - Static and dynamic power dissipation
  - AC parameters
    - Operating frequency
    - Timing parameters
    - Waveform presentation of timing parameters
  - Mechanical data
    - Package figure with pin assignment
    - Package dimensions
- Abbreviations