APPENDIX 2 - PLD EQUATIONS

MECFIX - IC9

```
MODULE ic9_new
"
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"
"-------------------------------------------------------------------------------------------
"
  TITLE                         'Preliminary MEC support'
" File name:                    IC9_NEW.ABL
" ABEL unit:                    (Type)
" Purpose and functionality:    (Text)
" Reference:                    (RDx)
" Analysis Dependencies:        (N/A)
" Limitations:                  (N/A)
" Fidelity:                     (N/A)
" Discrepancies:                (N/A)
" Usage:                        (N/A)
" I/O:                          (N/A)
" Operations:                   (N/A)
" Assertions:                   (N/A)
" Development Platform:         (N/A)
" Analyzer:                     (No Dependencies)
" Synthesis:                    (No Dependencies)
"
"-------------------------------------------------------------------------------------------
"
" Revision history:             (all revisions included)
"
"-------------------------------------------------------------------------------------------
" Version No:   Author:                         Mod. Date:  Changes made:
"-------------------------------------------------------------------------------------------
"       v1.0    Ola Persson                     951104      New issue
"       v2.0    Khalid Ismail                   960206      New work-around is implemented
"-------------------------------------------------------------------------------------------
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"-------------------------------------------------------------------------------------------
"
"
" This is an module that corrects the behaviour of the preliminary MEC
" Three errors in the MEC are fixed with this PLD
" - MDS_N / MEXC_N not asserted during store
" - MDS_N incorrectly asserted during INULL/FNULL cycle
" - Inserting one extra hold cycle to emulate the missing second store
"   cycle when a synchronous trap is taken according to FAX/ERC32/0080.(cpki)
" device type
ic9_new device 'p22v10';

" Input Signals
CLK             pin 1;
RESERVED1       pin 2;
RESERVED2       pin 3;
RESERVED3       pin 4;
INULL           pin 5;
FNULL           pin 6;
RD              pin 7;
MHOLD_N         pin 8;
MDS_N           pin 9;
FLUSH           pin 10;
" Output Signals

RESERVED4       pin 23 istype 'reg,pos';
RESERVED5       pin 22 istype 'reg,pos';
RESERVED3       pin 21 istype 'reg,pos';

INT_MHOLD_N     pin 20 istype 'reg,pos';
NEW_INULL       pin 19 istype 'reg,pos';
NEW_FNULL       pin 18 istype 'reg,pos';
NEW_MDS_N       pin 17 istype 'reg,pos';
MASK_MDS_N      pin 16 istype 'reg,pos';
RD_LATCH        pin 15 istype 'reg,pos';
NEW_MHOLD_N     pin 14 istype 'reg,pos';

equations

RESERVED3.OE = 0;
RESERVED4.OE = 0;
RESERVED5.OE = 0;

MASK_MDS_N.CLK = CLK;
MASK_MDS_N := !MHOLD_N & MASK_MDS_N
            #  MHOLD_N & FLUSH;

NEW_MDS_N.OE = 1;
NEW_MDS_N = MDS_N # MASK_MDS_N;
```

```
RD_LATCH.CLK = CLK;
RD_LATCH := RD;

NEW_INULL.OE = 1;
NEW_INULL = INULL & RD_LATCH;

NEW_FNULL.OE = 1;
NEW_FNULL = FNULL & RD_LATCH;

" internal MHOLD
INT_MHOLD_N.OE = 1;
INT_MHOLD_N.CLK = CLK;
INT_MHOLD_N := NEW_MHOLD_N;

" New MHOLD signal
NEW_MHOLD_N.OE = 1;
NEW_MHOLD_N.CLK = CLK;
NEW_MHOLD_N := !(FLUSH & !RD_LATCH) & (MHOLD_N # (NEW_MHOLD_N & INT_MHOLD_N));


END ic9_new
```

ATACIF - IC 48

```
MODULE ic48
"
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"-------------------------------------------------------------------------------------------------
"
  TITLE                         'Ada Tasking Accelerator Coprocessor Interface'
" File name:                    ATACIF.ABL
" ABEL unit:                    (Type)
" Purpose and functionality:    (Text)
" Reference:                    (RDx)
" Analysis Dependencies:        (N/A)
" Limitations:                  (N/A)
" Fidelity:                     (N/A)
" Discrepancies:                (N/A)
" Usage:                        (N/A)
" I/O:                          (N/A)
" Operations:                   (N/A)
" Assertions:                   (N/A)
" Development Platform:         (N/A)
" Analyzer:                     (No Dependencies)
" Synthesis:                    (No Dependencies)
"
"-------------------------------------------------------------------------------------------------
"
" Revision history:             (all revisions included)
"
"-------------------------------------------------------------------------------------------------
" Version No:     Author:                                 Modification Date:  Changes made:
"-------------------------------------------------------------------------------------------------
"       v1.0      Jörgen Jost auf der Stroth              940428              New issue
"       v1.1      Jörgen Jost auf der Stroth    940915                  Added signal BUSERR_N
"       v1.1      Jörgen Jost auf der Stroth    940920                  Removed signal ALE_N
"                                                                               Logical behavior and START
"                                                                               replaced by IOBEN_N
"                                                     950119                    PIN Placement
"       v2.0    Ola Persson                      951114              Statemachine rewritten
"                                                                    for DEM32 board
"-------------------------------------------------------------------------------------------------
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"-------------------------------------------------------------------------------------------------
"
"
" This is an module that interfaces a system with ready controlled accesses to the
" ATAC (Ada Tasking Accellerator Coprocessor).
"
" device type
ic48 device 'p22v10';

                                            " Input Signals
CLK             pin 1;
IOWR_N          pin 3;
SEL_N           pin 4;
RELEASE         pin 6;

                                            " Output Signals

CE_N            pin 23 istype 'reg,pos';
RD              pin 22 istype 'reg,pos';
WR_N            pin 21 istype 'reg,pos';

BUSRDY_N        pin 20 istype 'reg,pos';

BUSERR_N        pin 19 istype 'reg,pos';

Q1              pin 18 istype 'reg,pos';
Q2              pin 17 istype 'reg,pos';

States = [Q1,Q2,CE_N];

IDLE       = [0,0,1]; " No strobes active waiting for IOSEL_N negative
READ1      = [1,1,0]; " Waiting for RELEASE from ATAC or IOSEL_N positive
READ2      = [0,1,0]; " Goto READ2
READ3      = [1,0,0]; " Goto WAIT
WRITE1     = [0,0,0]; " Waiting for RELEASE from ATAC or IOSEL_N positive
WRITE2     = [1,0,1]; " Goto WRITE3
WRITE3     = [1,1,1]; " Goto WAIT
WAIT       = [0,1,1]; " No strobes active waiting for IOSEL_N positive

equations

States.clk      = CLK;


RD = Q1.fb # Q2.fb;
WR_N =  Q1.fb # Q2.fb;
BUSRDY_N = ((States.fb == READ1) # (States.fb == WRITE1) # (States.fb == IDLE)) ;
```

```
" BUSERR is not used
BUSERR_N = 1;

state_diagram States;
state IDLE:
   if ( !SEL_N & IOWR_N ) then " Start read access
      goto READ1;
   else if ( !SEL_N & !IOWR_N ) then " Start write access
      goto WRITE1;
   else
      goto IDLE;

state READ1:
   if RELEASE then " Waiting for RELEASE from ATAC
      goto READ2;
   else if SEL_N then  " If no cycle then IDLE
      goto IDLE;
   else
      goto READ1;  " Else wait here

state READ2:
   goto READ3;

state READ3:
   goto WAIT;

state WRITE1:
   if RELEASE then " Waiting for RELEASE from ATAC
      goto WRITE2;
   else if SEL_N then  " If no cycle then IDLE
      goto IDLE;
   else
      goto WRITE1; " Else wait here

state WRITE2:
   goto WRITE3;

state WRITE3:
   goto WAIT;

state WAIT:
   if !SEL_N then
      goto WAIT;
   else
      goto IDLE;


END ic48
```