PRELIMINARY

Ultra37000™ ISR™ CPLD Family

UltraLogic™ High-Performance CPLDs

Features

- **In-System Reprogrammable (ISR™) CMOS CPLDs**
  - **—JTAG interface for reconfigurability**
  - **—Design changes don't cause pinout changes**
  - **—Design changes don't cause timing changes**
- **High density**
  - **—32 to 512 macrocells**
  - **—32 to 256 I/O pins**
  - **—5 Dedicated Inputs including 4 clock pins**
- **High speed - 222 MHz in-system operation**
  - **—t_{PD} = 5 ns**
  - **—t_S = 2.5 ns**
  - **—t_{CO} = 3.5 ns**
- **Simple timing model**
  - **—No fanout delays**
  - **—No expander delays**
  - **—No dedicated vs. I/O pin delays**
  - **—No additional delay through PIM**
  - **—No penalty for using full 16 product terms**
  - **—No delay for steering or sharing product terms**
- **3.3-V and 5-V versions**
- **Fully PCI compliant[1]**
- **Bus Hold capabilities on all I/Os**
- **Intelligent product term allocator provides:**
  - **—0 to 16 product terms to any macrocell**
  - **—Product term steering on an individual basis**
  - **—Product term sharing among local macrocells**
- **Flexible clocking**
  - **—4 synchronous clocks per device**
  - **—Product Term clocking**
  - **—Clock polarity control**
- **Consistent package/pinout offering across all densities**
  - **—Same pinout for 3.3-V and 5-V devices**
  - **—Simplifies design migration across density**
- **Security bit and user ID supported**
- **Packages**
  - **—44 to 352 pins in PLCC, PQFP, TQFP, and BGA packages**
- ***Warp2*®**
  - **—Low-cost IEEE 1076/1164-compliant VHDL system**
  - **—Available on PC, Sun, and HP platforms for $99**
  - **—Supports all Cypress Programmable Products**
- ***Warp2*Sim™ adds:**
  - **—Capabilities of *Warp2* and Viewlogic's ViewSim**
  - **—Dynamic timing solutions for all Cypress PLDs**
- ***Warp3*® CAE development system adds:**
  - **—VHDL input**
  - **—Viewlogic graphical user interface**
  - **—Schematic capture (ViewDraw™)**
  - **—VHDL simulation (SpeedWave™)**

General Description

The Ultra37000™ family of CMOS CPLDs provides a range of high-density programmable logic solutions with unparalleled system performance. The Ultra37000 family is designed to bring the flexibility, ease of use, and performance of the 22V10 to high-density CPLDs. The architecture is based on a number of logic blocks that are connected by a Programmable Interconnect Matrix (PIM). Each logic block features its own product term array, product term allocator, and 16 macrocells. The PIM distributes signals from the logic block outputs and all input pins to the logic block inputs. *Figure 1* shows a block diagram of the Ultra37128.

All of the Ultra37000 devices are electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The ISR feature provides the ability to reconfigure the devices without having design changes cause pinout or timing changes. The Cypress ISR function is implemented through a JTAG-compliant serial interface. Data is shifted in and out through the TDI and TDO pins, respectively. Because of the superior routability and simple timing model of the Ultra37000 devices, ISR allows users to change existing logic designs while simultaneously fixing pinout assignments and maintaining system performance.

The entire family features JTAG for ISR and boundary scan, and is fully compliant with the PCI Local Bus specification, meeting all the electrical and timing requirements. The Ultra37000 family features bus-hold capabilities on all I/Os.

Ultra37000 Selection Guide

Device	Pins	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
Ultra37032/V	44	32	5	32	5	222
Ultra37064/V	44/84/100	64	5	32/64/64	6.5	167
Ultra37128/V	84/100/160	128	5	64/64/128	6.5	167
Ultra37192/V	160	192	5	120	7.5	154
Ultra37256/V	160/208/256	256	5	128/160/192	7.5	154
Ultra37384/V	208/256	384	5	160/192	10	125
Ultra37512/V	208/256/352	512	5	160/192/256	10	125

Shaded area contains advance information.

Note:

1. Due to the 5-V tolerant nature of the I/Os, the I/Os are not clamped to V_{CC}.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM provides extremely robust interconnection to avoid fitting and density limitations.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic blocks. Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the Ultra37000 family.

An important feature of the PIM is its simple timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. As a result, there are no route-dependent timing parameters on the Ultra37000 devices. The worst-case PIM delays are incorporated in all appropriate Ultra37000 specifications.

Routing signals through the PIM is completely invisible to the user. All routing is accomplished by software—no hand routing is necessary. *Warp* and third-party development packages automatically route designs for the Ultra37000 family in a matter of minutes. Finally, the rich routing resources of the Ultra37000 family accommodate last minute logic changes while maintaining fixed pin assignments.

Logic Block

The logic block is the basic building block of the Ultra37000 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used.

Product Term Array

Each logic block features a 72 x 87 programmable product term array. This array accepts 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 87 product terms in the array can be created from any of the 72 inputs.

Of the 87 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining seven product terms in the logic block are output enable (OE) product terms. Each of the OE product terms controls up to eight of the 16 macrocells and is selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block.

Logic Block Diagram

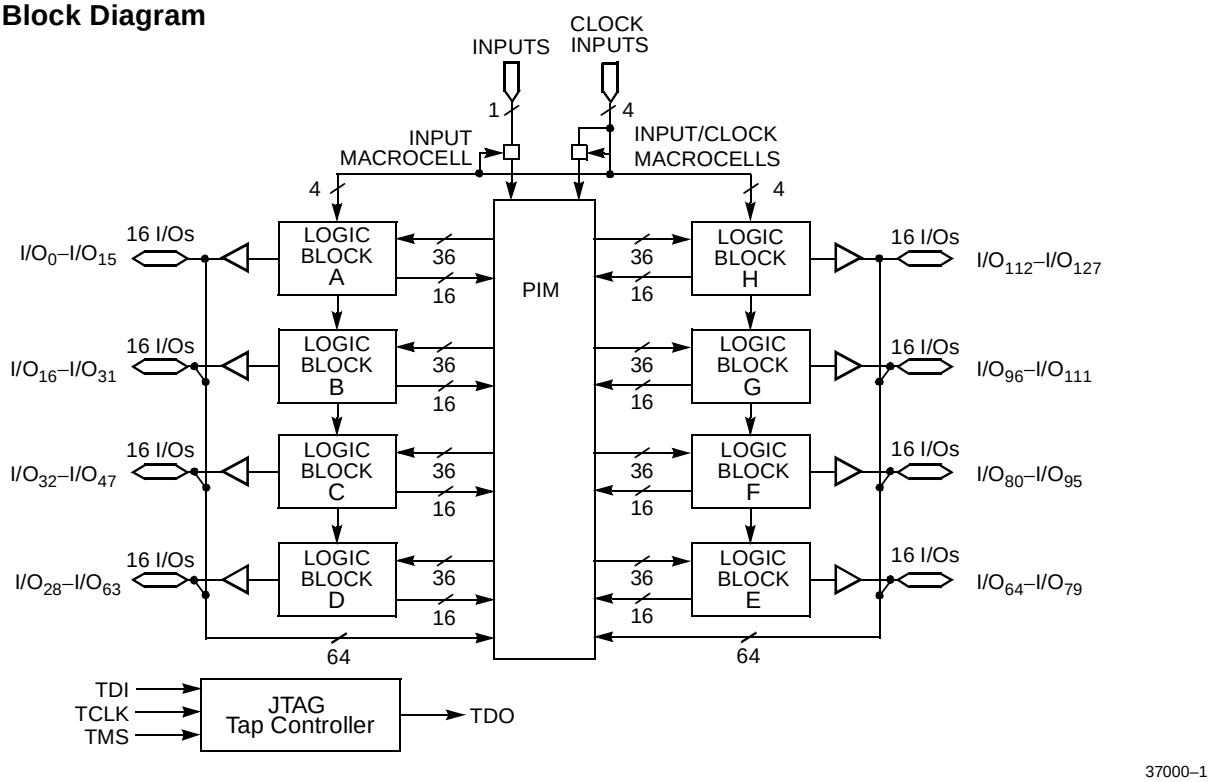

Figure 1. Ultra37128 Block Diagram

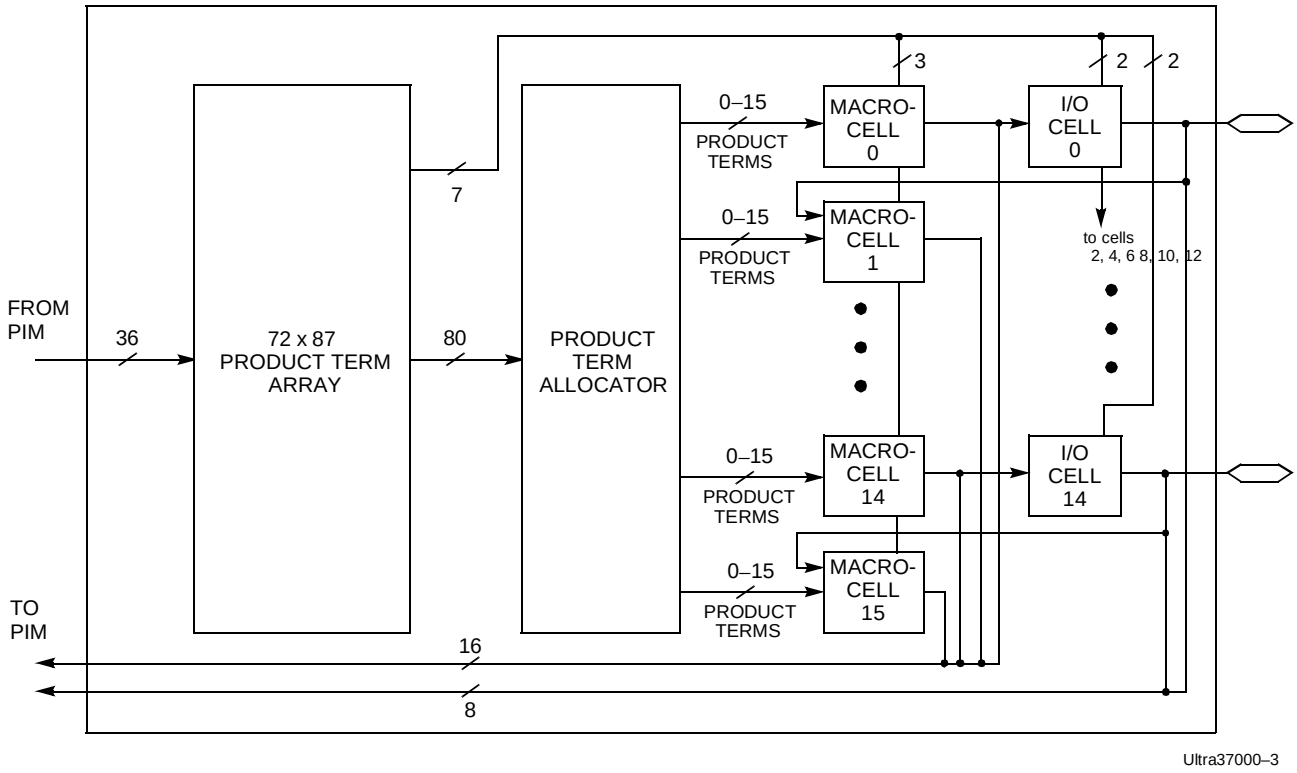

Figure 2. Logic Block with 50% Buried Macrocells

The next two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms. The final product term is the product term clock. The set, reset, OE and product term clock have polarity control to realize OR functions in a single pass through the array.

Product Term Allocator

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

Product Term Steering

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

Product Term Sharing

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

Low Power Option

Each logic block can operate in high speed mode for critical path performance, or in low power mode for power conservation. The logic block mode is set by the user on a logic block by logic block basis.

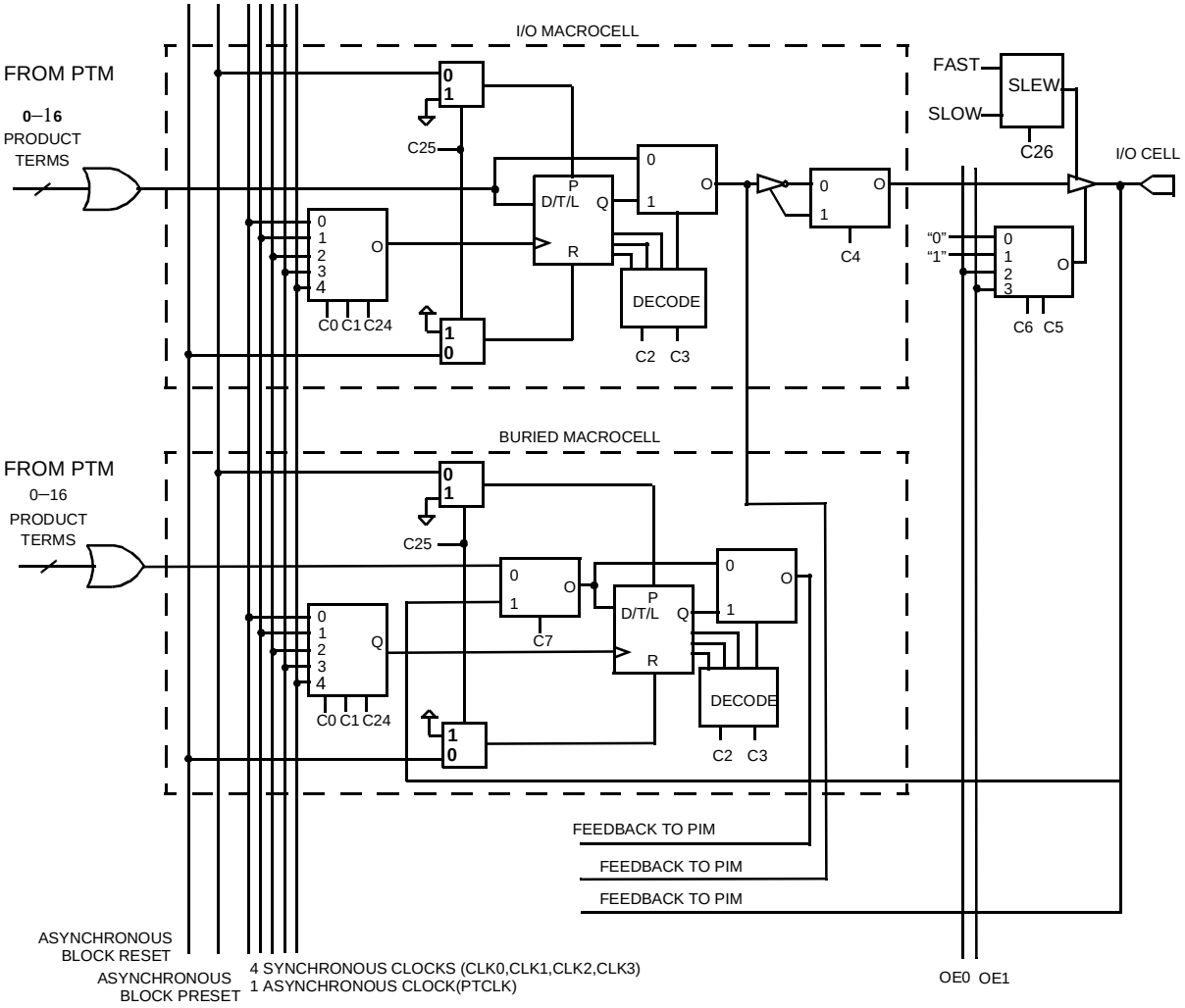

Figure 3. I/O and Buried Macrocells

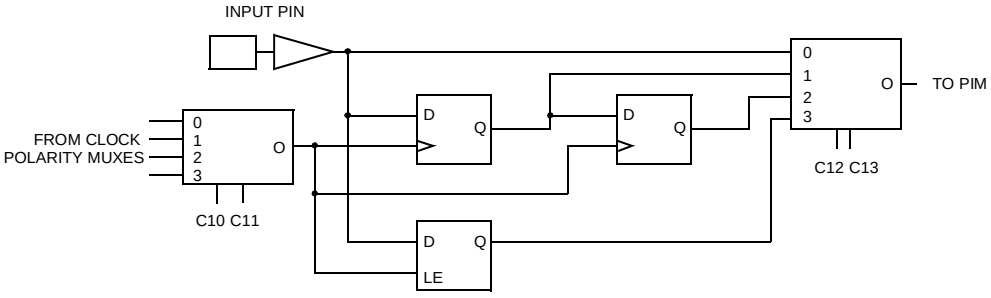

Figure 4. Input Macrocell

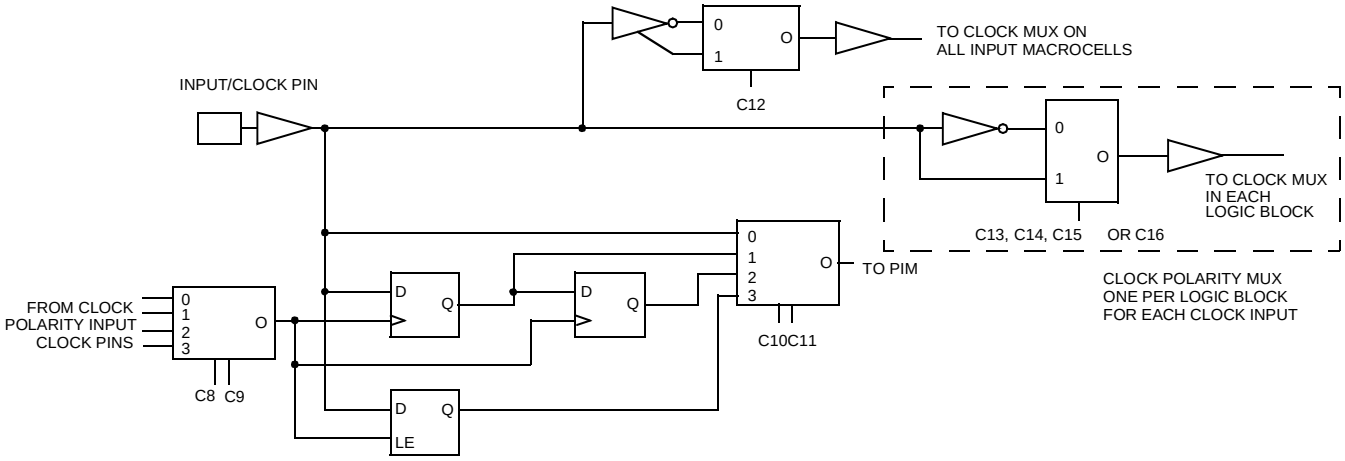

Figure 5. Input/Clock Macrocell

Ultra37000 Macrocell

Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

Buried Macrocell

Figure 3 displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.

The buried macrocell also supports input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

I/O Macrocell

Figure 3 illustrates the architecture of the I/O macrocell. The I/O macrocell supports the same functions as the buried macrocell with the addition of I/O capability. At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

The Ultra37000 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

Bus Hold Capabilities on all I/Os

Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND. For more information see the application note "Understanding Bus-hold – A Feature of Cypress CPLDs".

Programmable Slew Rate Control

Each output has a programmable configuration bit, which sets the output slew rate to fast or slow. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.

Ultra37000 5-V Devices

The Ultra37000 devices operate with a 5-V supply, can support 5-V or 3.3-V I/O levels. V_{CCO} connections provide the capability of interfacing to either a 5-V or 3.3-V bus. By connecting the V_{CCO} pins to 5-V the user insures 5-V TTL levels on the outputs. If V_{CCO} is connected to 3.3-V the output levels meet 3.3-V JEDEC standard CMOS levels and are 5-V tolerant. These devices require 5-V ISR programming.

Ultra37000V 3.3-V Devices

Devices operating with a 3.3-V supply require 3.3-V on all V_{CCO} pins, reducing the device's power consumption. These devices support 3.3-V JEDEC standard CMOS output levels, and are 5-V tolerant. These devices allow 3.3-V ISR programming.

PCI Compliance

5-V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3-V products meet all PCI requirements except for the output 3.3-V clamp, which is in direct conflict with 5-V tolerance. The Ultra37000 family's simple and predictable timing

model ensures compliance with the PCI AC specifications independent of the design.

IEEE 1149.1 Compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode and Usercode boundary scan instructions. The JTAG interface is shown in *Figure 6*.

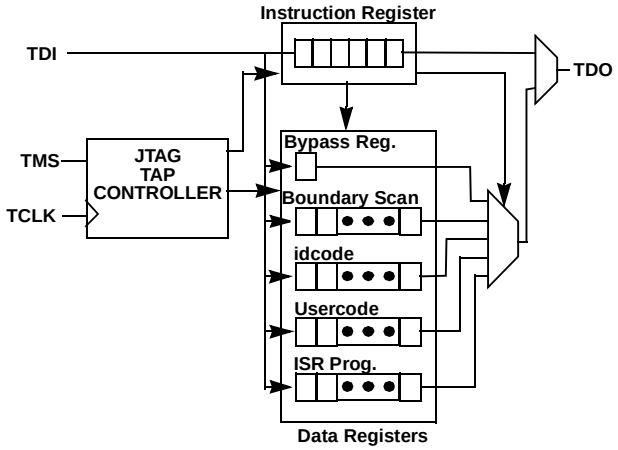

Figure 6. JTAG Interface

In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexability, and a simple timing model for consistent system performance.

Clocking

Each I/O and buried macrocell has access to 4 synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all 4 synchronous clocks.

Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 4* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 5 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

Product Term Clocking

In addition to the 4 synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independant product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 7* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5–ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

The Ultra37000 features:

- no fanout delays
- no expander delays
- no dedicated vs. I/O pin delays
- no additional delay through PIM
- no penalty for using 0-16 product terms
- no added delay for steering product terms
- no added delay for sharing product terms
- no routing delays
- no output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.

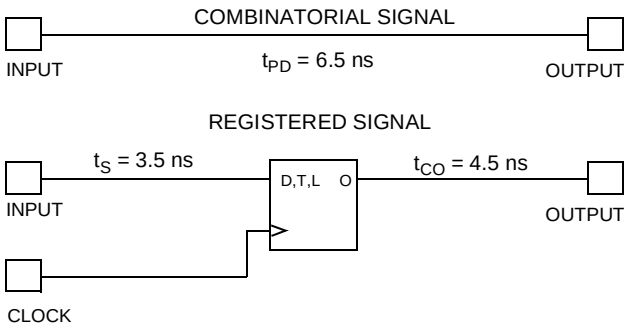

Figure 7. Timing Model for Ultra37128

Development Software Support

Warp2®

Warp2 is a state-of-the-art VHDL compiler for designing with Cypress programmable logic. *Warp2* utilizes IEEE 1076/1164 VHDL as the Hardware Description Language (HDL) for design entry. VHDL provides a number of significant benefits for design entry. *Warp2* accepts VHDL input, synthesizes and optimizes the entered design, and outputs a JEDEC map for the desired Ultra37000 device. For simulation, *Warp2* provides a graphical waveform simulator as well as VHDL and Verilog Timing Models.

VHDL (VHSIC Hardware Description Language) is an open, powerful, non-proprietary language that is a standard for behavioral design entry and simulation. VHDL allows designers to learn a single language that is useful for all facets of the design process. See the *Warp2* data sheet for further information.

Warp3®

Warp3 is a sophisticated development system that is based on the latest version of Viewlogic's CAE design environment. *Warp3* features schematic capture (ViewDraw™), VHDL waveform simulation (SpeedWave™), a VHDL debugger, and VHDL synthesis, all integrated in a graphical design environment. *Warp3* is available on PCs using Windows 3.1, Windows95 or Windows NT and on Sun and Hewlett Packard workstations. See the *Warp3* data sheet for further information.

*Warp2*Sim™

This development system combines the capabilities of *Warp2* and Viewlogic's ViewSim™ package which provides dynamic timing solutions for all Cypress programmable logic devices.

Third-Party Software

Cypress products are supported in a number of third party design entry and simulation tools. All major third-party software vendors (including ABEL™, Synario, LOG/iC™, CUPL™, Mentor, etc.) provide support for the Ultra37000 family of devices. Refer to the third party software data sheet or contact your local sales office for a list of currently supported third party vendors.

Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the InSRkit ISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The ISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on Cypress ISR Interface, see the ISR Programming Kit.

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). Contact your local sales office for information on availability of this option.

The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the InSRkit data sheets.

The *Impulse3*™ device programmer from Cypress will program all Cypress programmable logic devices, as well as USB, PROM and EPROM products. This unit is a programmer that connects to any IBM-compatible PC via the printer port. For further information see the *Impulse3* data sheet.

Third-Party Programmers

As with development software, Cypress support is available on a wide variety third-party programmers. All major third-party programmers (including Data I/O, Logical Devices, Minato, SMS, and Stag) support the Ultra37000 family.

Document #: 38–00475–B