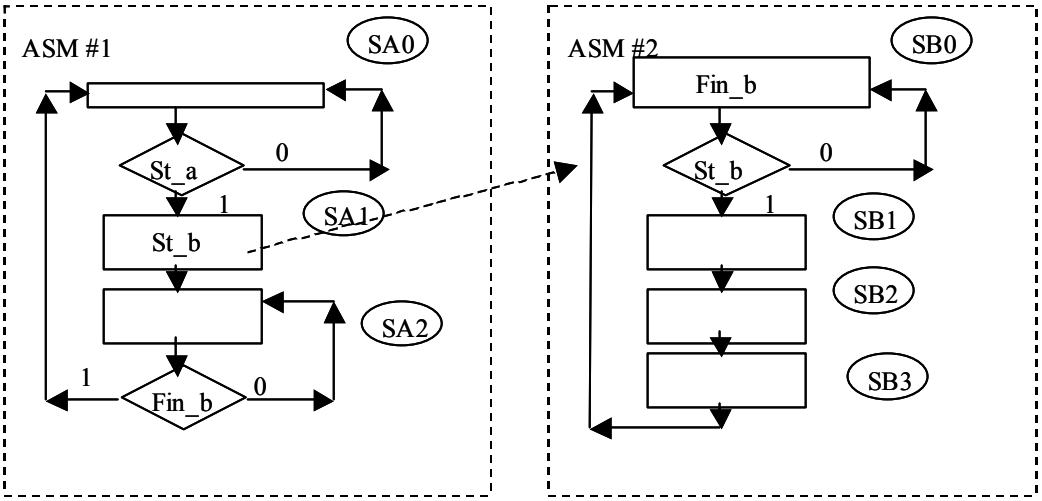
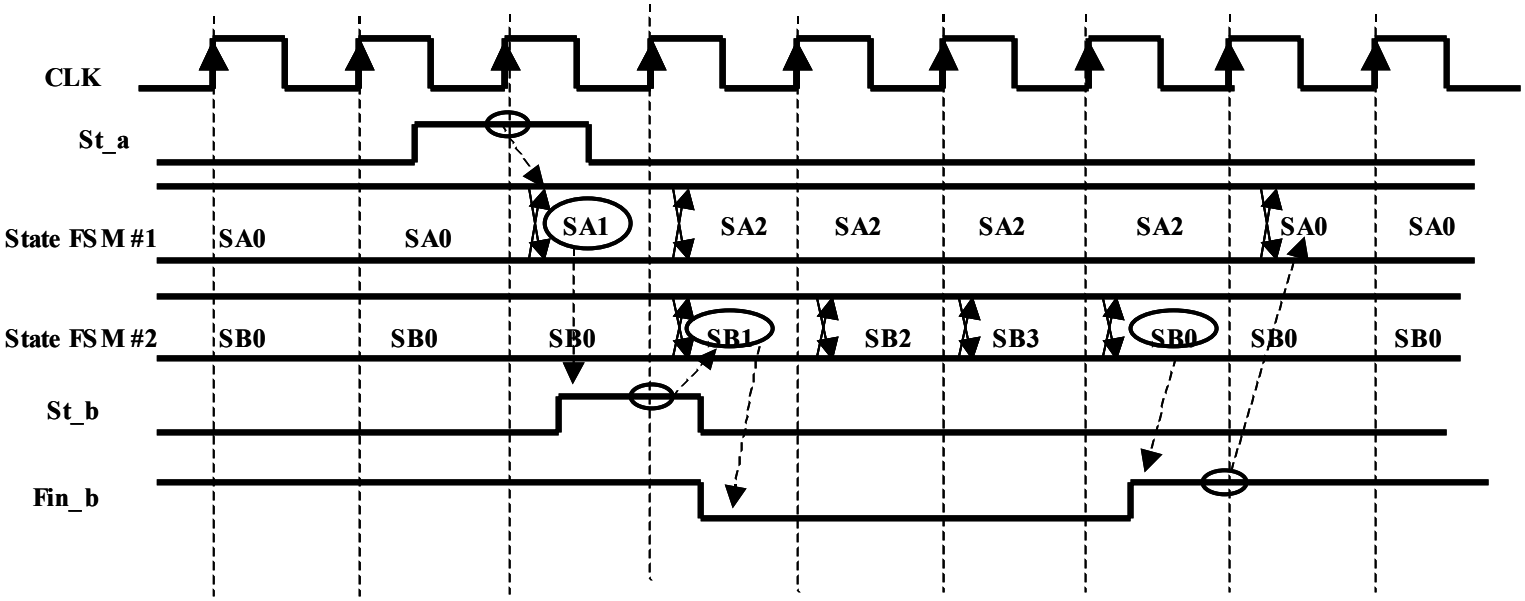
EE 4743 Test #3 Solutions – Fall 2002

For any partial credit, you must show your work.

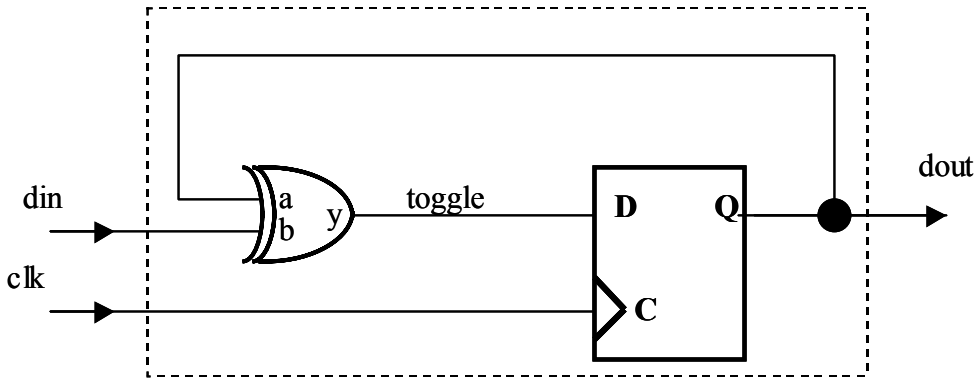
1. **(20** pts) Fill out all clock cycles for the timing diagram shown below for the cooperating finite state machines shown below:





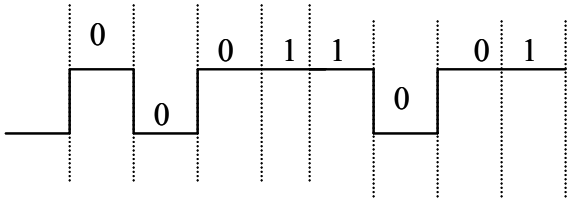
2. **(15** pts) Draw the schematic resulting from the following structural VHDL. Label all pins, nets. Indicate the inputs/outputs to the top level schematic. Draw nets between pins of components to connect them – don' t just label them.

```
library IEEE;
use IEEE.std_logic_1164.all;

entity test is
  port (    din, clk: in std_logic;
            dout: out std_logic
            );
end test;

architecture a of test is
  component dff is
     port ( d,clk: in std_logic;
            q: out std_logic  );
   end component;

  component xor2 is
     port ( a,b: in std_logic;
            y : out std_logic  );
   end component;
  signal toggle: std_logic;

  begin
    u1: xor2
       port map (a => dout,
                         b => din,
                         y => toggle
                         );

    u2: dff
       port map (d => toggle,
                    clk => clk,
                   q => dout
                         );

  end a;
```



You may skip THREE of the remaining 16 questions. Cross out the THREE questions that you do not want me to grade.

3. In class, we discussed NRZI encoding that is used by USB. Draw the waveform for sending the 8-bit value 98H (10011000), send it LSB first. Assume that the initial value of the serial line is a LOW voltage.



4. What did 'bit-stuffing' mean in conjunction with the USB protocol?

   Inserted a '0' bit if six consecutive '1' bits was sent

5. Why was 'bit-stuffing' and NRZI encoding used with the USB protocol?

   To allow the receiver to maintain synchronization to the bit stream.

6. What is a **fault** in digital circuit? Name two types of faults.

   A fault is a manufacturing defect in either an interconnect or transistor.

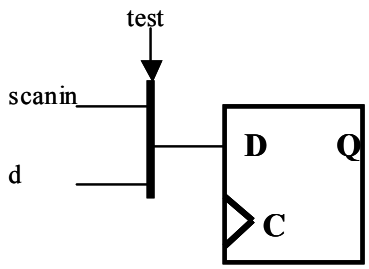
   Three types of faults are stuck-at-0, stuck-at-1, or stuck-open.

7. In design for test, we discussed two types of 'abilities' that are needed to improve "test-ability". What are these?

   controllability, observability

8. What is a scannable D-Flip-Flop? Draw a schematic.

   It is a DFF with a mux in front of it.



9. What does the following code in Verilog synthesize to:

```
always (posedge clk)
   if (r==1) q = 0
      else q = d;
```

A D-flip-flop with a synchronous reset.

10. What does BIST mean?

    Built-In-Self-Test – circuitry is added to a digital system so that it can test itself

11. What would a LFSR be used in for in a BIST scheme?

    To generate test vectors for the BIST

12. What did IEEE 1149.1 (JTAG) specify? Be specific.

    A standard method for putting IO pins on an ASIC in a scan path. The standard also allowed for internal DFFs to be placed on the scan path. This allows all ASICs on a board to be inserted in a single scan path for board-level testing.

13. In class I mentioned that Verilog was better for low-level modeling. Why is this?

Verilog has built-in gate-level and transistor-level primitives in the language specification.

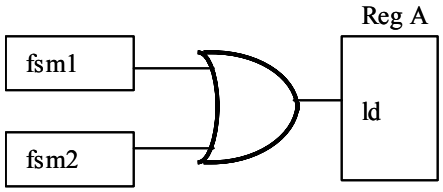
14. How do you compute the number of lines per screen for a raster scan display given the dot clock frequency, the horizontal sync frequency, and the vertical synch frequency?

    # of lines = horizontal sync freq / vertical sync freq

15. In structural VHDL that specifies an Altera LPM component, how do you pass a parameter value to the component?

    *Via the **generic map** in the instantiation of the component.*

16. Draw a small schematic that shows how two FSMs might both be able to assert the load line to a register.



17. What is the primary goal in automated test vector pattern generation?

    To obtain the highest fault coverage with the fewest vectors.

18. In class, we discussed that processors integrated into high-end FPGAs were becoming common. What does it mean if a processor is a 'soft macro' in an FPGA? What is the advantage of this? What is a disadvantage (and you CANNOT use 'not(your_advantage)').

A soft macro is a processor that is specified in RTL and synthesized to the programmable elements of the FPGA. The advantage is that this provides flexibility – for example, the size of the datapath could be a parameter (16 bits versus 32 bits). The disadvantage is that this will be slower than a hard macro and take up more silicon area.