E2 – Framing / Deframing according ITU-T G.703 / G.742 : VHDL-Modules

Standard : ITU-T G.703 and G.742
Datarate : 8448 kbit/sec
Tolerance : +/- 30 ppM

Bit number 1 to 212

Set 1 to 4	212 Bits
	212 Bits
	212 Bits
	212 Bits

Bit number 1 to 212

Set 1 to 4	FAS 1111010000	RAI	Na	200 Payload Bits
	Justification Control Bits Cj1	208 Payload Bits		
	Justification Control Bits Cj2	208 Payload Bits		
	Justification Control Bits Cj3	Justification Payload Bits Jj		204 Payload Bits

Bit number 1 to 212

Set 1 to 4	F1	F1	F1	F1	F0	F1	F0	F0	F0	F0	RAI	Na	200 Payload Bits
	C11	C21	C31	C41	208 Payload Bits								
	C12	C22	C32	C42	208 Payload Bits								
	C13	C23	C33	C43	J1	J2	J3	J4	204 Payload Bits				

The E2 transmission scheme according G.742 consists of frames with a length of 848 bits. A frame consists of four sets, which are 212 bits long. 9962.26 frames are transmitted per second.

Frame synchronization is achieved, if three consecutive correct frame alignment signals are detected. Frame synchronization is lost, if four consecutive defective frame alignment signals are detected.

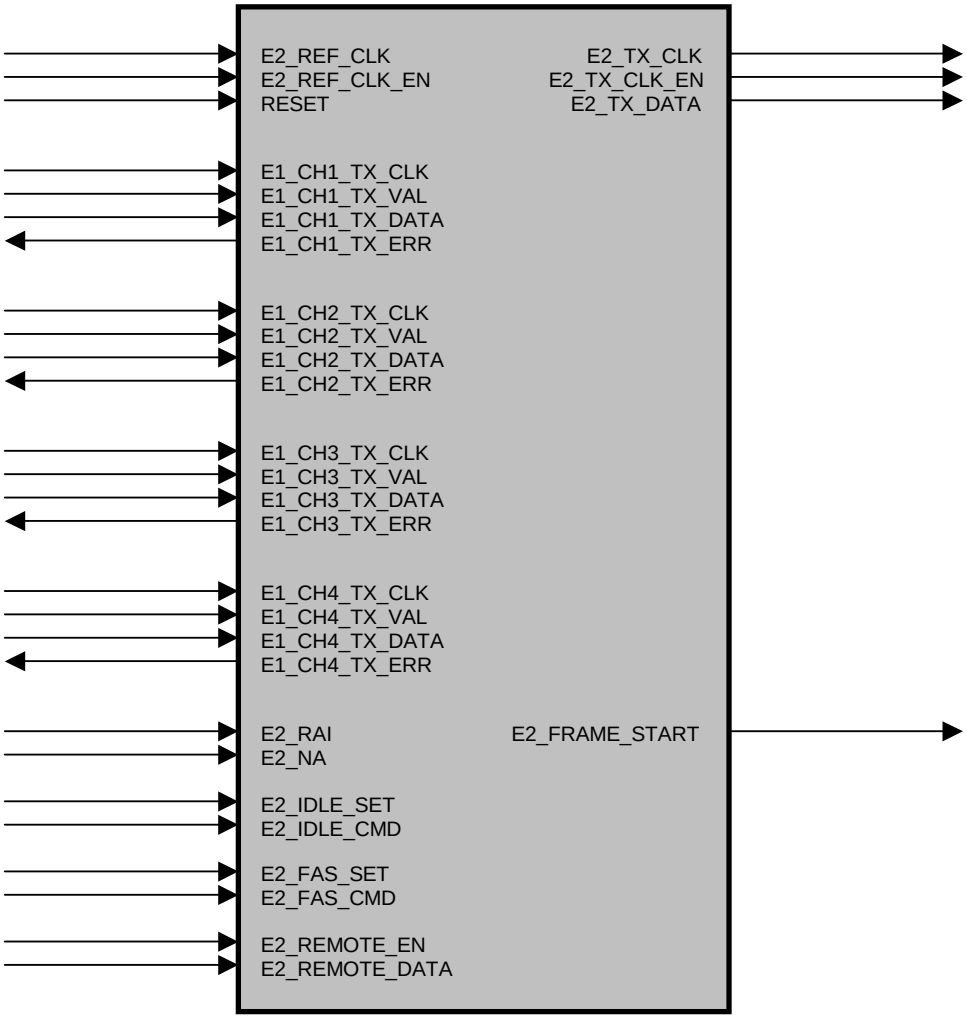
The Frame Alignment Signal (FAS) is located in the first set of a frame. The Remote Alarm Indication (RAI) Bit and the National (NA) Bit are following the FAS. The remainder of the first set is filled with the four E1 data streams. These data streams are mapped in a bit interleaved manner, starting with the first E1 data stream. There is no frame alignment between the multiplex formats E2 and E1.

Only positive justification is used. The first four bits in the sets two to four are the justification control bits (C_{JN}). The justification payload or stuffing bits (J_J) are located in the forth set in the bits five to eight. The justification control bits specifies if the corresponding justification payload bits are carrying valid data bits or not.

The receiver performs the following majority-decision :
A valid data bit is transmitted in the justification payload bit (J_J) if no or one bit in the corresponding justification bit sequence (C_{J1}, C_{J2}, C_{J3}) is set.
No valid data bit is transmitted in the justification payload bit (J_J) if two or three bits in the corresponding justification bit sequence (C_{J1}, C_{J2}, C_{J3}) are set.

The nominal data rate of E1 is 2048 kbit/sec. The E2 payload inclusive the justification payload bits can transport per E1 channel 2052.2 kbit/sec. Without the justification payload bits the transport capacity per E1 channel is 2042.3 kbit/sec. The justification payload bits are used to transport data with a utilisation of 57.6 % at the nominal E1 data rate of 2048 kbit/sec.

E2-Framer-Module



Framer : VHDL-Entity

```
entity E2_G742_FRAMER is
  port (
    E2_REF_CLK     : in  std_logic;                     -- Framer Clock
    E2_REF_CLK_EN  : in  std_logic;                     -- Framer Clock Enable
    RESET          : in  std_logic;                     -- Reset
    E1_CH1_TX_CLK  : in  std_logic;                     -- E1 Channel 1 Clock
    E1_CH1_TX_VAL  : in  std_logic;                     -- E1 Channel 1 Data Valid
    E1_CH1_TX_DATA : in  std_logic;                     -- E1 Channel 1 Data
    E1_CH1_TX_ERR  : out std_logic;                     -- E1 Channel 1 Error-Out
    E1_CH2_TX_CLK  : in  std_logic;                     -- E1 Channel 2 Clock
    E1_CH2_TX_VAL  : in  std_logic;                     -- E1 Channel 2 Data Valid
    E1_CH2_TX_DATA : in  std_logic;                     -- E1 Channel 2 Data
    E1_CH2_TX_ERR  : out std_logic;                     -- E1 Channel 2 Error-Out
    E1_CH3_TX_CLK  : in  std_logic;                     -- E1 Channel 3 Clock
    E1_CH3_TX_VAL  : in  std_logic;                     -- E1 Channel 3 Data Valid
    E1_CH3_TX_DATA : in  std_logic;                     -- E1 Channel 3 Data
    E1_CH3_TX_ERR  : out std_logic;                     -- E1 Channel 3 Error-Out
    E1_CH4_TX_CLK  : in  std_logic;                     -- E1 Channel 4 Clock
    E1_CH4_TX_VAL  : in  std_logic;                     -- E1 Channel 4 Data Valid
    E1_CH4_TX_DATA : in  std_logic;                     -- E1 Channel 4 Data
    E1_CH4_TX_ERR  : out std_logic;                     -- E1 Channel 4 Error-Out
    E2_RAI         : in  std_logic;                     -- Remote Alarm Indication
    E2_NA          : in  std_logic;                     -- National Bit
    E2_FRAME_START : out std_logic;                     -- Frame Pulse
    E2_IDLE_SET    : in  std_logic;                     -- Pulse : new IDLE Command
    E2_IDLE_CMD    : in  std_logic_vector (2 downto 0); -- IDLE Command
    E2_FAS_SET     : in  std_logic;                     -- Pulse : new FAS Command
    E2_FAS_CMD     : in  std_logic_vector (2 downto 0); -- FAS Command
    E2_REMOTE_EN   : in  std_logic;                     -- Remote Channel : Enable
    E2_REMOTE_DATA : in  std_logic_vector (3 downto 0); -- Remote Channel : TX Data
    E2_TX_CLK      : out std_logic;                     -- E2 Output Clock
    E2_TX_CLK_EN   : out std_logic;                     -- E2 Output Clock Enable
    E2_TX_DATA     : out std_logic                      -- E2 Output Data
  );
end E2_G742_FRAMER;
```

Framer : Interface Description

E2_REF_CLK

Base clock for the E2 framer. The whole E2 logic of the framer works with this clock.

E2_REF_CLK_EN (E2_REF_CLK synchronous)

Clock enable input for the framer. Set to 1 when using a 8.448 MHz clock. Used when working with a higher clock (like 34.368 MHz) which is used as a single clock for a greater system.

RESET

Asynchronous reset for the whole internal logic (E2 and the four E1 domains) of the framer.

E1_CH1_TX_CLK / E1_CH2_TX_CLK / E1_CH3_TX_CLK / E1_CH4_TX_CLK

Clock for the E1 TX interface channels. Could be asynchronously regarding to the other E1 channels. The nominal data rate is 2048 kbit/sec.

E1_CH1_TX_VAL / E1_CH2_TX_VAL / E1_CH3_TX_VAL / E1_CH4_TX_VAL

Clock enable input for the E1 TX interface channel. Set to 1 when using a 2.048 MHz clock. Used when working with a higher clock (like 34.368 MHz) which is used as a single clock for a greater system. When this input is at 1 during the rising edge on the corresponding channel clock input, the data bit at the corresponding channel data input is registered in the input FIFO.

E1_CH1_TX_DATA / E1_CH2_TX_DATA / E1_CH3_TX_DATA / E1_CH4_TX_DATA

User data input for the E1 TX channel interface. A data bit is sampled with the rising edge on the corresponding channel clock input.

E1_CH1_TX_ERR / E1_CH2_TX_ERR / E1_CH3_TX_ERR / E1_CH4_TX_ERR

Error signal output for the E1 TX interface. If the channel FIFO detects a overflow or underflow this error is reported by a 1 signal for the duration of the error.

E2_RAI (E2_REF_CLK synchronous)

Remote Alarm Indication input. The bit at this input is sampled at the frame begin and transmitted as RAI bit in the E2 frame.

E2_NA (E2_REF_CLK synchronous)

National Bit input. The bit at this input is sampled at the frame begin and transmitted as NA bit in the E2 frame.

E2_FRAME_START (E2_REF_CLK synchronous)

This signaling output notifies the begin (first bit) of one frame. It reports this event by a 1 signal for a clock period (plus clock enable).

E2_IDLE_SET (E2_REF_CLK synchronous)

Command input. The framer assumes the command word at the E2_IDLE_CMD input with a pulse for one clock period. The execution of this command is done at the next frame begin.

E2_IDLE_CMD (E2_REF_CLK synchronous)

0 0 0 : normal operation
0 1 0 : transmit ‚0' during frame payload
0 1 1 : transmit ‚1' during frame payload
1 0 0 : transmit idle signal ‚0' (unframed)
1 0 1 : transmit idle signal ‚1' (unframed)

E2_FAS_SET (E2_REF_CLK synchronous)

Command input. The framer assumes the command word at the E2_FAS_CMD input with a pulse for one clock period. The execution of this command is done at the next frame begin.

E2_FAS_CMD (E2_REF_CLK synchronous)

0 0 0 : normal operation
0 1 0 : transmit one defective FAS, only one bit error : 1111000000 instead of 1111010000
0 1 1 : transmit one defective FAS, all bits inverted : 0000101111 instead of 1111010000
1 0 0 : transmit four consecutive FAS, only one bit error : 1111000000 instead of 1111010000
1 0 1 : transmit four consecutive FAS, all bits inverted : 0000101111 instead of 1111010000

E2_REMOTE_EN (E2_REF_CLK synchronous)

Activation input for the data transfer channel to the remote device. Set to 0 if not used.

E2_REMOTE_DATA (E2_REF_CLK synchronous)

Data transfer channel to the remote device. These four bits wide channel is transmitted in the E2 frame overhead instead of the first four justification control bits (C_{J1}). It's possible because the receiver performs a majority-decision with the three justification control nibbles (C_{J1},C_{J2},C_{J3}) when deciding if a justification must be done or not. One erroneous nibble doesn't affect the justification decision.
The transmit rate in this channel is 9962.26 nibbles per second or 39849 bit/sec. The nibble at this input is sampled at the frame begin.

E2_TX_CLK

Clock Output (derived from E2_REF_CLK) to the line interface.

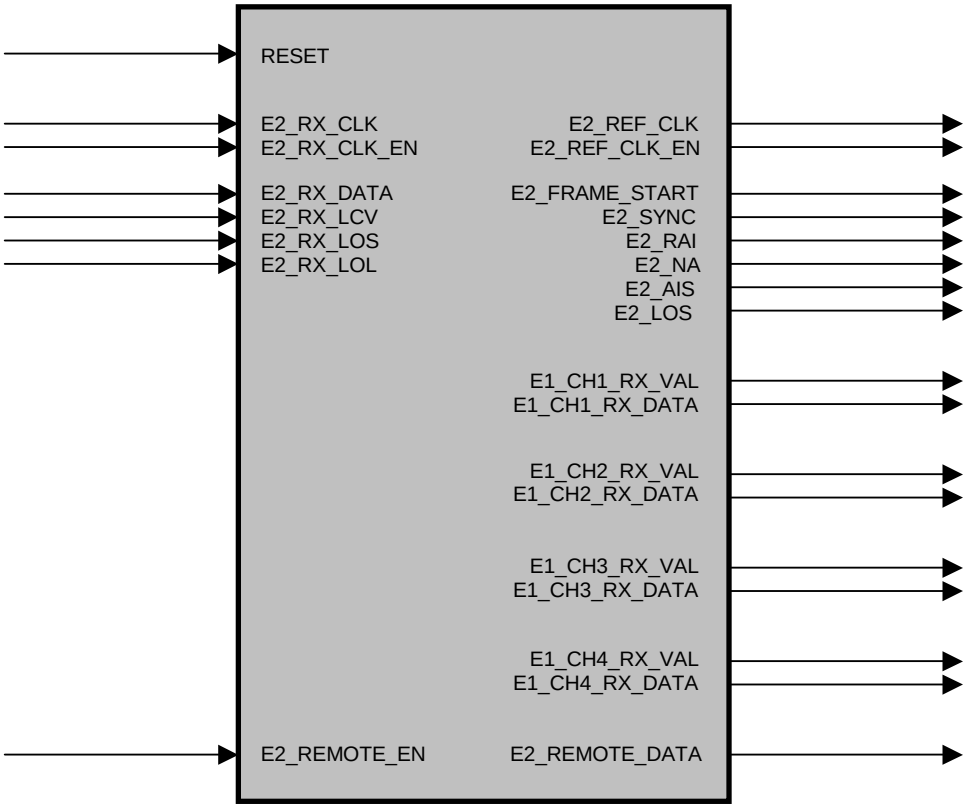
E2_TX_CLK_EN (E2_TX_CLK synchronous)

Clock Enable Output (derived from E2_REF_CLK_EN) to the line interface. E2_TX_DATA is valid only when E2_TX_CLK_EN is high.

E2_TX_DATA (E2_TX_CLK synchronous)

Serial E2 data output to the line interface.

E2-Deframer-Module



Deframer : VHDL-Entity

```
entity E2_G742_DEFRAMER is
  port (
    RESET          : in  std_logic;                     -- Reset
    E2_RX_CLK      : in  std_logic;                     -- RX Input Data Clock
    E2_RX_CLK_EN   : in  std_logic;                     -- RX Input Data Clock Enable
    E2_RX_DATA     : in  std_logic;                     -- RX Input Data
    E2_RX_LCV      : in  std_logic;                     -- RX Code Violation
    E2_RX_LOS      : in  std_logic;                     -- RX Loss Of Signal
    E2_RX_LOL      : in  std_logic;                     -- RX Loss Of Lock
    E2_REF_CLK     : out std_logic;                     -- Output Ref. Clock
    E2_REF_CLK_EN  : out std_logic;                     -- Output Ref. Clock Enable
    E2_FRAME_START : out std_logic;                     -- Frame Pulse
    E2_SYNC        : out std_logic;                     -- State : Frame Synchronous
    E2_RAI         : out std_logic;                     -- State : RAI Bit
    E2_NA          : out std_logic;                     -- State : NA Bit
    E2_AIS         : out std_logic;                     -- State : Alarm Ind. Signal
    E2_LOS         : out std_logic;                     -- State : Loss Of Signal
    E1_CH1_RX_VAL  : out std_logic;                     -- E1 Channel 1 Data Valid
    E1_CH1_RX_DATA : out std_logic;                     -- E1 Channel 1 Data
    E1_CH2_RX_VAL  : out std_logic;                     -- E1 Channel 2 Data Valid
    E1_CH2_RX_DATA : out std_logic;                     -- E1 Channel 2 Data
    E1_CH3_RX_VAL  : out std_logic;                     -- E1 Channel 3 Data Valid
    E1_CH3_RX_DATA : out std_logic;                     -- E1 Channel 3 Data
    E1_CH4_RX_VAL  : out std_logic;                     -- E1 Channel 4 Data Valid
    E1_CH4_RX_DATA : out std_logic;                     -- E1 Channel 4 Data
    E2_REMOTE_EN   : in  std_logic;                     -- Remote Channel : Enable
    E2_REMOTE_DATA : out std_logic_vector (3 downto 0)  -- Remote Channel : RX Data
  );
end E2_G742_DEFRAMER;
```

Deframer : Interface Description

RESET

Asynchronous reset for the whole internal logic of the deframer.

E2_RX_CLK

Receive clock for the E2 deframer. The whole logic of the deframer works with this clock.

E2_RX_CLK_EN

Clock enable input for the deframer. Set to 1 when using a 8.448 MHz clock. Used when working with a higher clock (like 34.368 MHz) which is used as a single clock for a greater system.

E2_RX_DATA

Serial RX data stream for the E2 deframer.

E2_RX_LCV

Line Code Violation (received data bit is invalid because violation of the coding rules).

E2_RX_LOS

Loss Of Signal (No receive signal available).

E2_RX_LOL

Loss Of Lock (Receive signal frequency beyond the CDR frequency range).

E2_REF_CLK

Output of the E2 reference clock (Derived from E2_RX_CLK).

E2_REF_CLK_EN

Output of the clock enable signal (E2_RX_CLK_EN). Used when working with a higher frequency than 8,448 MHz.

E2_FRAME_START (E2_REF_CLK Synchronous)

This signaling output notifies the reception (first bit) of a frame. It reports this event by a 1 signal for a clock period (plus clock enable).

E2_SYNC (E2_REF_CLK Synchronous)

Synchronization state output.
This output changes to 1 if three consecutive frames with error free frame alignment signals are received. It changes to 0 if four consecutive frames with errored frame alignment signals are received.

E2_RAI (E2_REF_CLK Synchronous)

Remote Alarm Indication output.
This output changes to 1 if the received RAI bits in the last four frames are at 1. It changes to 0 if the received RAI bits in the last four frames are at 0. The output is immediately updated, when the RAI bit is received. If the frame synchronization is lost, this output is reset to 0.

E2_NA (E2_REF_CLK Synchronous)

National Bit output.
The level at this output reflects the level of the received NA bit. The output is immediately updated, when the NA bit is received. If the frame synchronization is lost, this output is reset to 0.

E2_AIS (E2_REF_CLK Synchronous)

State output signal : Receiving Alarm Indication Signal (Idle '1').
The AIS output changes to 1 if four or less 0 bits are detected during the last two frame periods (2x 848 bits). The AIS output changes to 0 if five or more 0 bits are detected during the last two frame periods (2x 848 bits) or when frame synchronization could be achieved.

E2_LOS (E2_REF_CLK Synchronous)

State output signal : Receiving Loss Of Signal (Idle '0').
The LOS output changes to 1 if the inputs E2_RX_LOS or E2_RX_LOL changes to 1 or if 128 consecutive 0 bits are received. The LOS output changes to 0 if the inputs E2_RX_LOS and E2_RX_LOL are at 0 and if at least one 1 bit was received in the last 128 received bits.

E1_CH1_RX_VAL / E1_CH2_RX_VAL / E1_CH3_RX_VAL / E1_CH4_RX_VAL

Receive data valid signal for the corresponding channel data output. Synchronized at the clock E2_REF_CLK. The nominal data rate for E1 is 2048 kbit/sec.

E1_CH1_RX_DATA / E1_CH2_RX_DATA / E1_CH3_RX_DATA / E1_CH4_RX_DATA

Receive channel data output. Synchronized at the clock E2_REF_CLK.

E2_REMOTE_EN (E2_REF_CLK Synchron)

Activation input for the data transfer channel from the remote device. Set to 0 if not used.

E2_REMOTE_DATA (E2_REF_CLK Synchron)

Data transfer channel from the remote device. These four bits wide channel is transmitted in the E2 frame overhead instead of the first four justification control bits (C_{J1}). A nibble with new data is provided with every new frame, which can be noticed by the E2_FRAME_START signal.