Assignment # 4
March 7th, 2007
Due: March 16th, 2007, 9pm.

The purpose of this assignment is an introduction to synthesis using the Xilinx tools.

1 Warm-Up

You can download the Xilinx 9.1 ISE tools from
http://www.xilinx.com/ise/logic_design_prod/webpack.htm.

Run through the Quickstart tutorial that can be accessed from the Help menu. Stop on page 24 before "Assigning Pin Location Constraints". Print and attach the signal trace from the behavioral simulation.

2 Main Assignment

This Assignment has two parts

2.1 Simple Synthesis Walkthrough

Design and implement an 8-bit hierarchical ALU (built from single bit ALUs (you can use the one created in Assignment 2). Target one of the Virtex components for your design. Report on

1. The maximum clock frequency
2. Area requirements in terms of the number of slices and flip flops.
3. Attach the map and translate reports available from the design summary. What do map and translate do?

2.2 Familiarization with the 1076.6 Standard

The IEEE 1076.6 Standard establishes the RTL subset of VHDL. Go through this standard to answer the following questions.

1. Which logic operations are not supported?
2. Are both inertial and transport delay models acceptable inputs for a model to be compliant?
3. Are unconstrained arrays supported?
4. What forms of the wait statement, if any are supported?

3 Submission Instructions:

Name the files using the convention from the last assignment and zip all files into a compressed folder, and email to **mbales3@gatech.edu** by 9 pm on the due date. Place 4170 Assignment 4 in the subject line.