XAPP702 (v1.0) September 10, 2004

DDR-2 Controller Using Virtex-4 Devices

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Summary

DDR-2 SDRAM devices offer new features that go beyond the DDR SDRAM specification and enable a DDR-2 device to operate at data rates of 400 Mb/s and above. High data rates demand higher performances from the controller and the I/Os in the FPGA. It is essential for the controller to operate synchronously with the operating speed of the memory to achieve the desired bandwidth.

Introduction

This application note describes a 267 MHz DDR-2 controller implementation in a Virtex-4™ device interfacing to a Micron DDR-2 SDRAM device. This document provides a brief overview of the DDR-2 SDRAM device features followed by a detailed explanation of the controller operation when interfacing to high-speed DDR-2 memories. It also explains the back-end user interface to the controller. Reference designs in Verilog are available for download from the Xilinx web site.

DDR-2 SDRAM Device Overview

DDR-2 SDRAM devices are the next generation DDR devices. DDR-2 SDRAM devices use the SSTL 1.8V I/O standard. The following section explains the features available in the DDR-2 SDRAM devices and the key differences between DDR SDRAM and DDR-2 SDRAM devices.

DDR-2 SDRAM devices use a DDR architecture to achieve high-speed operation. The memory operates using a differential clock provided by the controller. Commands are registered at every positive edge of the clock. A bi-directional data strobe (DQS) is transmitted along with the data for use in data capture at the receiver. DQS is a strobe transmitted by the DDR-2 SDRAM device during reads, and by the controller during writes. DQS is edge-aligned with data for reads, and center-aligned with data for writes.

Read and write accesses to the DDR-2 SDRAM device are burst oriented; accesses begin with the registration of an active command, and then followed by a read or write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed. The address bits registered with the read or write command are used to select the bank and the starting column location for the burst access.

The DDR-2 controller design includes a user back-end interface that generates the write address, write data, and the read addresses. This information is stored in four asynchronous FIFOs for address and data synchronization between the back-end and controller modules. Based on the availability of data in the FIFOs and the commands issued by the command logic block, the controller issues the correct commands to the memory, taking into account the timing requirements of the memory. The implementation details of the logic blocks are explained in the following sections.

DDR-2 Commands Issued by the Controller

Table 1 lists the commands issued by the controller. The commands are detected by the memory using the following control signals:

- Row Address Select ($\overline{RAS}$)
- Column Address Select ($\overline{CAS}$)
- Write Enable ($\overline{WE}$) signals
- Clock Enable (CKE) is held High throughout and after device configuration
- Chip Select ($\overline{CS}$) is held Low throughout device operation

Table 1: **DDR-2 Commands**

Selection	Function	Row Address Select	Column Address Select	Write Enable Signals
1	Load Mode	L	L	L
2	Auto Refresh	L	L	H
3	Precharge(1)	L	H	L
4	Bank Activate	L	H	H
5	Write	H	L	L
6	Read	H	L	H
7	No Operation/IDLE	H	H	H

Notes:

1. Address signal A10 is held High during PRECHARGE ALL BANKs and is held Low during single bank precharge.

The following sections explain the functions of the DDR-2 commands supported by the controller.

Mode Register

The mode register is used to define the specific mode of operation of the DDR-2 SDRAM. This includes the selection of burst length, burst type, CAS latency, and operating mode. Figure 1 shows the features of the mode register used by the controller.

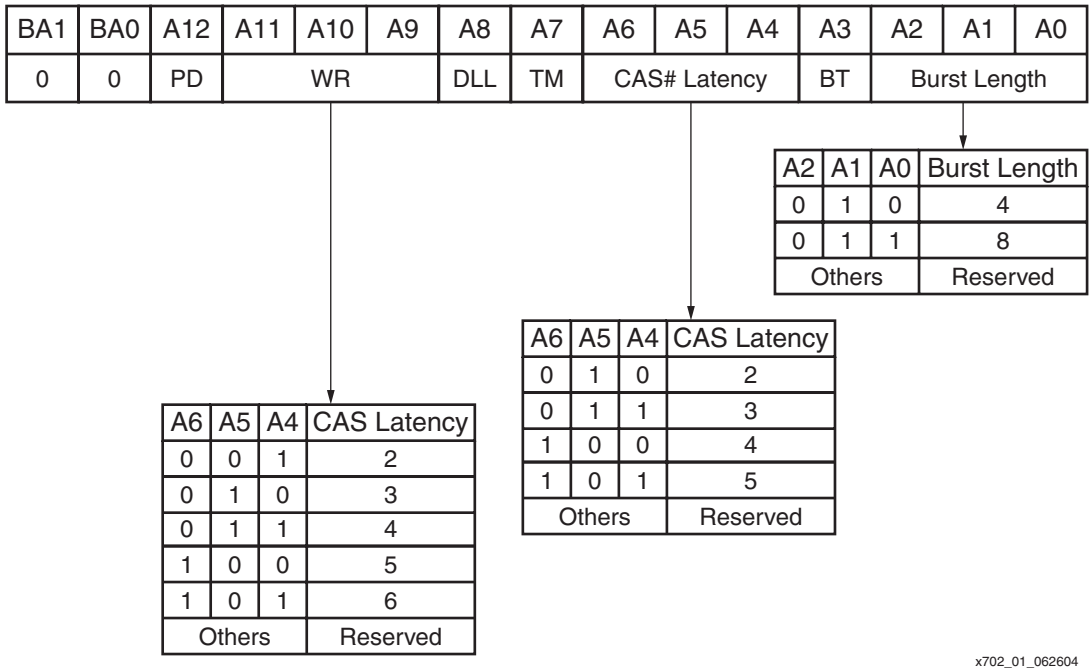

Figure 1: **Mode Register**

Bank addresses BA1 and BA0 select the mode registers. Table 2 shows the configuration of the bank address bits.

Table 2: **Bank Address Bit Configuration**

BA1	BA0	Mode Register
0	0	Mode Register (MR)
0	1	EMR1
1	0	EMR2
1	1	EMR3

Extended Mode Register

The extended mode register controls functions beyond those controlled by the mode register. As shown in Table 3, these additional functions are DLL enable/disable, output drive strength, on-die termination (ODT), posted CAS additive latency (AL), off-chip driver impedance calibration (OCD), $\overline{DQS}$ enable/disable, RDQS/$\overline{RDQS}$ enable/disable, and output disable/enable.

Table 3: **Extended Mode Register**

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	Out	RDQS	$\overline{DQS}$	OCD program			R_{TT}	Posted CAS			R_{TT}	ODS	DLL

The DDR-2 SDRAM reference design uses an AL of 0. OCD is not used in this design.

Extended Mode Register 2 (EMR2)

Bank addresses are set to `10`, where BA1 is High and BA0 is Low. The address bits are all set Low.

Extended Mode Register 3 (EMR3)

Bank address bits are set to `11`, where BA1 and BA0 are High. The address bits are all set Low.

Initialization Sequence

The initialization sequence used in the controller state machine follows the DDR-2 SDRAM specifications. The memories voltage requirements must be met by the interface.The clock enable (CKE) signal must be asserted High after FPGA configuration. The sequence of commands issued for initialization are:

1. Precharge ALL command
2. EMR2 command. BA0 is held Low, and BA1 is held High
3. EMR3 command. BA0 and BA1 are both held High.
4. EMR command to enable the memory DLL. BA1 and A0 are held Low, and BA0 is held High.
5. Mode register set command for DLL reset. 200 clock cycles are required to lock the DLL.
6. Precharge ALL command.
7. Two auto-refresh commands
8. Mode register set command with Low to A8

After this sequence is complete, the controller issues dummy reads to the DDR-2 SDRAM memory. The data path module uses the data strobe (DQS) issued by the memory during this dummy read period to determine the relationship between the incoming DQS and the internal system clock, CLK0. Once the data path module has determined tthe amount of delay required for the DQS to align with the system clock, it issues a TAP_SELECT_DONE signal to the controller. The controller then moves into the IDLE state and is now ready for normal operation.

Precharge Command

The precharge command is used to deactivate the open row in a particular bank. The bank will be available for a subsequent row activation a specified time (t_{RP}) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged.

Auto-Refresh Command

DDR-2 devices are required to be refreshed every 7.8 µs. The circuit to flag the auto-refresh command is built into the controller. The controller uses the DCMs CLKDV output for the refresh counter. When asserted, the AUTO_REF signal flags the need for auto-refresh commands. The AUTO_REF signal is held High for 7.8 µs after the previous auto-refresh command. The controller then issues the auto-refresh command once it has completed the transactions in the current open bank.

Active Command

Before any read or write commands can be issued to a bank within the DDR-2 SDRAM memory, a row in that bank needs to be activated using an active command. After a row has been opened, read or write commands can be issued to that row subject to the t_{RCD} specification. DDR-2 SDRAM devices also support posted CAS additive latencies (AL). They allow a read or a write command to be issued prior to the t_{RCD} specification, by delaying the actual registration of the read or write command to the internal device by AL clock cycles. The DDR-2 controller does not use the CAS additive latencies while issuing read or write commands following an active command.

When the controller detects an incoming address referring to a row in a bank other than the currently opened row, the controller issues an address conflict signal. The controller then issues a precharge command to deactivate the open row, and then issues another active command to the new row.

Read Command

The read command is used to initiate a burst read access to an active row. The value on BA0 and BA1 select the bank address and the address inputs provided on $A_0 – A_I$ select the starting column location. Once the read burst is over, the row will still be available for subsequent access until it is precharged.

Figure 2 shows the case of a read command with an additive latency (AL) of zero. Hence, the read latency in this case is the same as the CAS latency (CL = 3).

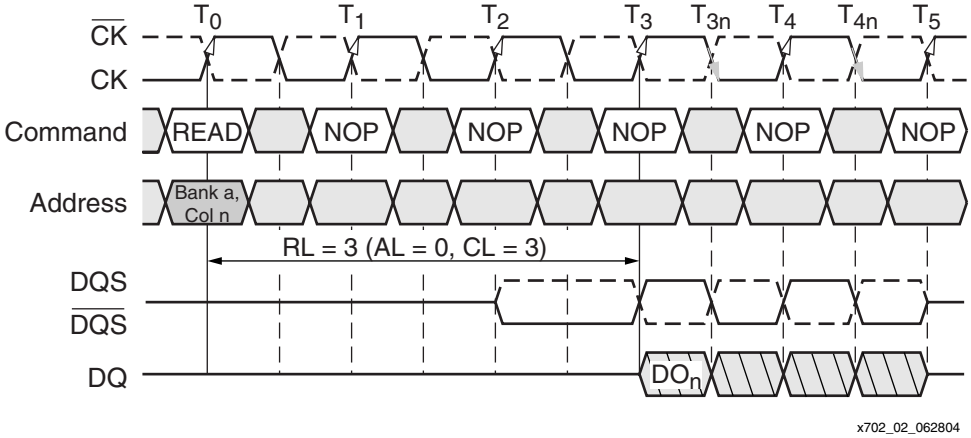

Figure 2: **Read Command Example**

Write Command

The write command is used to initiate a burst access to an active row. The value on BA0 and BA1 select the bank address, while the value on address inputs $A_0 – A_I$ select the starting column location in the active row. DDR-2 SDRAMs use a write latency (WL) equal to the read latency minus one clock cycle.

Write Latency = Read Latency – 1 = (Additive Latency + CAS Latency) – 1.

Figure 3 shows the case of a write burst with a write latency of two. The time between the write command and the first rising edge of the DQS signal is determined by the write latency.

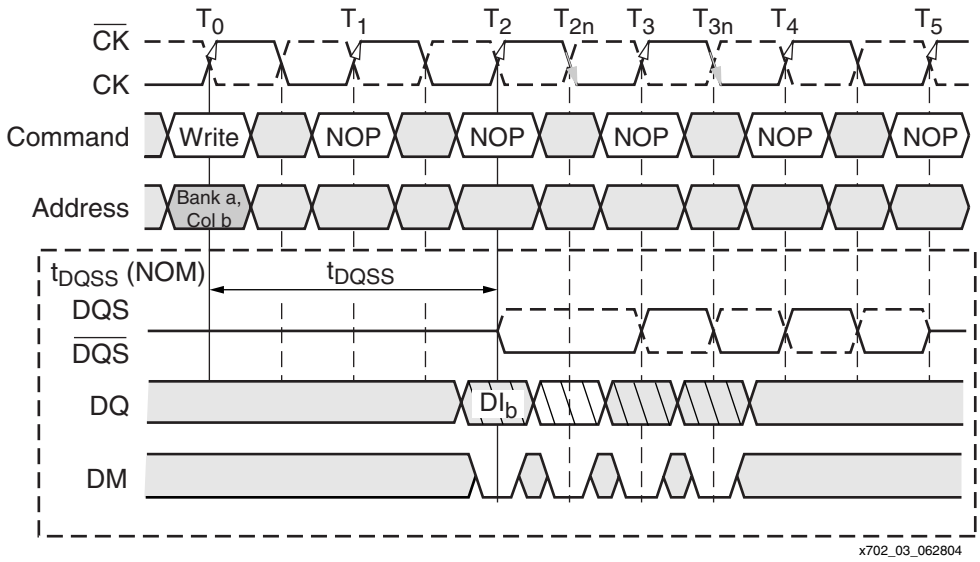

Figure 3: **Write Command Example**

DDR-2 Interface Implementation

The DDR-2 interface includes the blocks shown in Figure 4.

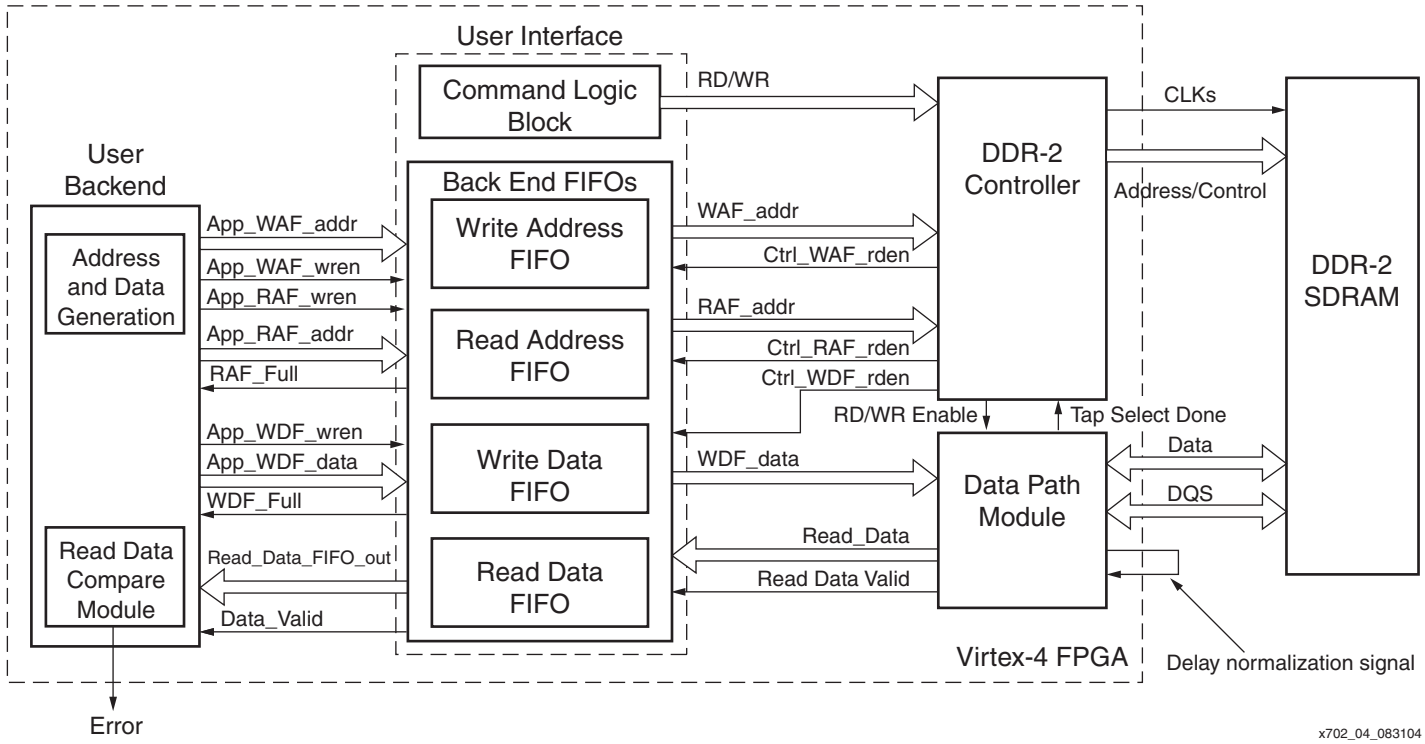

Figure 4: **DDR-2 Complete Interface**

User Back-end

The back-end of the reference design provides address and data patterns to test all the design aspects of a DDR-2 controller. The user back-end includes the following blocks: back-end state machine, read data comparator, and a data generator module. The data generation module generates the various address and data patterns that are written to the memory. The address

locations are pre-stored in a block RAM used as a ROM. The address values stored are selected to test accesses to different rows and banks in the DDR-2 SDRAM device. The data pattern generator includes a state machine issuing patterns of data. The back-end state machine replaces the user back-end. This issues the write or read enable signals to determine the FIFO to be accessed by the data generator module.

User Interface

The back-end user interface uses four FIFOs, the write-address FIFO, the write-data FIFO, the read address FIFO, and the read data FIFO. The first three FIFOs are accessed by the user backend modules. The read data FIFO is accessed by the data path module to store the captured read data.

Command Logic Block

The command logic block provides the commands to the controller. The user can modify this to their own command generation module or replace with a command FIFO. The command generation module used in the reference design generates alternate read and write commands. The command logic block is a simple state machine that issues commands to the controller. Figure 5 shows a state diagram of the command logic block.

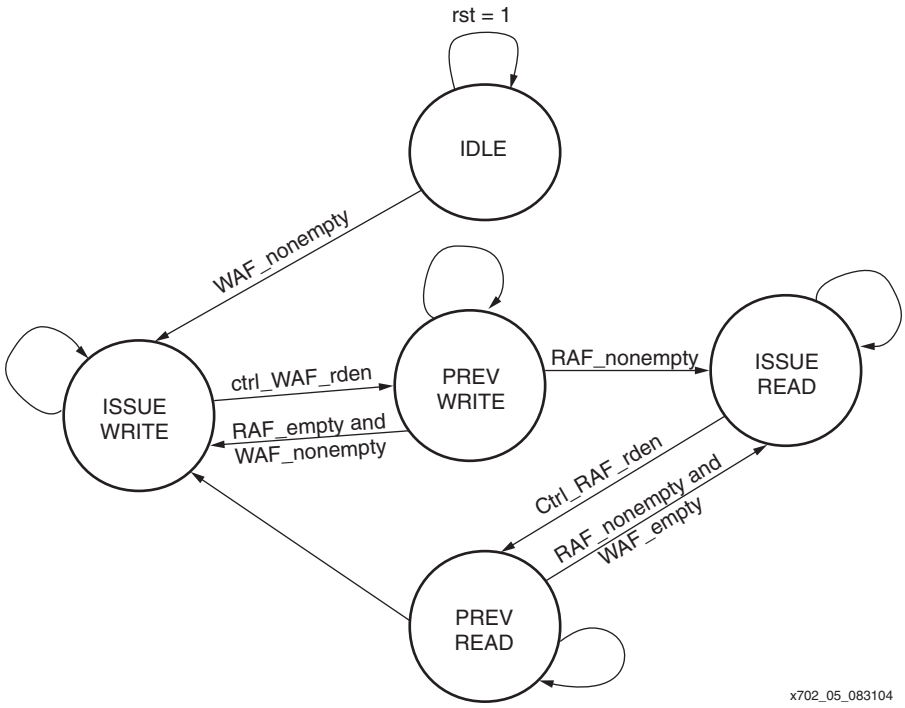

Figure 5: **Command Logic Block State Machine**

Controller Implementation

The controller state machine issues the commands in the correct order while considering the timing requirements of the memory. Figure 6 outlines the various stages in the controller state machine.

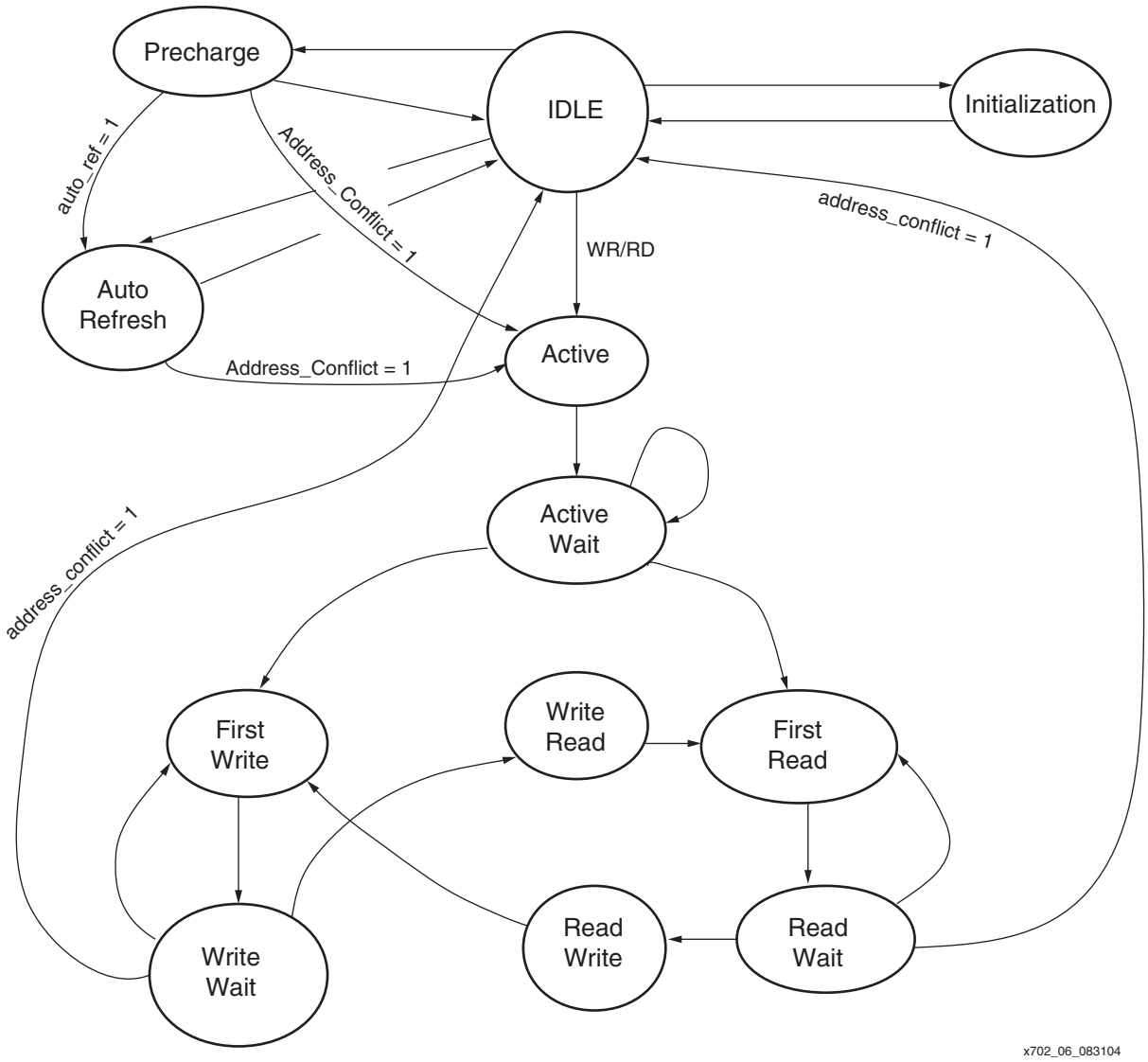

Figure 6: **DDR-2 Controller State Machine**

Before the controller issues commands to the memory:

1. The command logic block generates a write/read command.
2. The controller issues a read enable signal to the write/read address FIFO.
3. The controller activates a row in the corresponding bank if all banks have been precharged, or compares the bank and row addresses to the already open row and bank address. If there is a conflict, the controller precharges the open bank and then issues an active command before moving to the read/write states.
4. In the write state, if the controller detects a read command, the controller waits for the write_to_read time before issuing the read command. Similarly, in the read state, when the controller detects a write command from the command logic block, the controller waits for the read_to_write time before issuing the write command.
5. The commands are pipelined to synchronize with the address signals before being issued to the DDR-2 memory.

Conclusion

In this reference design, the utilization of the Virtex-4 DCM, IOB, and differential clock tree enable the DDR-2 controller to operate at the required speed.

Reference Design

The reference design for the DDR-2 controller using Virtex-4 devices is available on the Xilinx web site at www.xilinx.com/bvdocs/appnotes/xapp702.zip.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/10/04	1.0	Initial Xilinx release.