



TABLE 2—EDN PLD DIRECTORY: REPRESENTATIVE PALs, SPLDs, AND CPLDs

Product line and configuration technology (antifuse, EPROM, flash, PROM, ROM, SRAM, or other)	Core operating voltages (V)	Packaging and pincount options	Macrocell count	Number of macrocells per logic block/ number of inputs to each logic block	Logic-block interconnect approach (global or hierarchical)
Altera Max 3000A (EEPROM)	3.3	PLCC, PQFP, TQFP (44 to 208 pins)	32 to 256	16/36	Global
Max 7000AE (EEPROM)	3.3	0.8-mm BGA, 1-mm BGA, 1.27-mm BGA, PLCC, PQFP, TQFP (44 to 256 pins)	32 to 512	16/36	Global
Max 7000B (EEPROM)	2.5	0.8-mm BGA, 1-mm BGA, 1.27-mm BGA, PLCC, PQFP, TQFP (44 to 256 pins)	32 to 512	16/36	Global
Max 7000S (EEPROM)	5	PLCC, PQFP, RQFP, TQFP (44 to 208 pins)	32 to 256	16/36	Global
Atmel ATF15xx family (EEPROM)	3 to 3.6 (ASV/AE), 4.5 to 5.5 (AS/SE)	BGA 49/100/169/256, PLCC 44/84, PQFP 100/160/208, TQFP 44/100/144	32 to 256	16/40	Global
ATF16V8, ATF20V8, ATF22V10 (EEPROM)	3 to 5.5, 4.5 to 5.5	DIP 20/24, PLCC 20/28, SOIC 20/24, TSSOP 20/24	Eight to 10	NA	Global
ATF750 (EEPROM)	3 to 3.6, 4.5 to 5.5	DIP 24, PLCC 28, SOIC 24, TSSOP 24 DIP 40, LCC 44	10	NA	Global
ATF2500 (EEPROM)	4.5 to 5.5		24	NA	Global
Cypress Semiconductor Delta39K (SRAM)	1.8, 2.5, 3.3	FBGA 256/484/676, PQFP 208, self-boot BGA 388, self-boot FBGA 256/484/676	512 to 5376	16/36	Hierarchical
PSI (Programmable Serial Interface) (SRAM)	3.3	Self-boot BGA 456	1536 to 3072	16/36	Hierarchical
Quantum38K (SRAM)	2.5, 3.3	FBGA 256/484, PQFP 208	512 to 1536	16/36	Hierarchical
SPLD (EEPROM)	5	CDIP 20/24, CLCC 20/28, PDIP 20/24, PLCC 20/28	Eight, 10	Eight/16, eight/20, 10/22	Global
Ultra37000 (EEPROM)	3.3, 5	BGA 256/352, CLCC 44/84, CQFP 160/208, FBGA 48/100/256/400, PLCC 44/84, PQFP 208, TQFP 44/100/160	32 to 512	16/36	Global
Integrated Circuit Technology (ICT) PEEL Arrays (EEPROM)	4.75 to 5.25	DIP 24/28/40, PLCC 28/44, SOIC 24/28, TQFP 44, TSSOP 28	40 to 72	As many as 80 inputs/block	Global
PEEL Device (EEPROM)	4.75 to 5.25	DIP20/24, PLCC 20/28, SOIC 20/24, TSSOP 20/24	Eight to 10	As many as 22 inputs/block	Global
TPA (Tiny PEEL Arrays)	3	PDIP 8, SIP 8, SOIC 8, TSOP 8	10	As many as 32 inputs/block	Global
Zero Power PEEL Devices (EEPROM)	2.7 to 3.6, 4.75 to 5.25	DIP 20/24, PLCC 20/28, SOIC 20/24, TSSOP 20/24	Eight to 10	As many as 22 inputs/block	Global
Lattice Semiconductor 2000E (EEPROM)	5	PLCC 44, PQFP 128, TQFP 44/48/100/128/176	32 to 128	Four/18	Global
2000VE (EEPROM)	3.3	CABGA 49/100, FPBGA 144/208, PLCC 44, PQFP 160,	32 to 192	Four/18	Global

Embedded memory density (bits)	Size of each embedded memory block (bits)	Other embedded functions	Other notable features	Price range (end of 2001; 10,000 units; cheapest package; lowest speed; commercial temperature)
NA	NA		2.5V-, 3.3V-, and 5V-compatible I/O buffers, 4.5-nsec propagation delays, low-power mode, fast programming times, JTAG ISP support, PCI-compatible	\$1 to \$8
NA	NA		2.5V-, 3.3V-, and 5V-compatible I/O buffers, 4.5-nsec propagation delays, low-power mode, fast programming times, JTAG ISP support, PCI-compatible	\$1.40 to \$29
NA	NA		1.8V-, 2.5V-, and 3.3V-compatible I/O buffers, support for GTL+ and SSTL I/O standards, 3.5-nsec propagation delays, low-power mode, JTAG in-system-programmable support, PCI-compatible	\$1.40 to \$29
NA	NA		3.3V- and 5V-compatible I/O buffers, 6-nsec propagation delays, low-power mode, fast programming times, JTAG ISP support, PCI-compatible	\$3 to \$34
NA	NA		Logic-doubling density and routing enhancements, industry-standard pin compatibility, ISP through JTAG port, PCI compatible, low-standby-power input-transition detection (L and QL) versions	90 cents to \$10
NA	NA		Wide, battery-friendly operating-voltage range, quarter-power (Q) and low-standby-power input-transition detection (QL, Z and QZ) versions	40 cents to \$1
NA	NA		Two 22V10s in the same 24/28-pin package, low-standby-power input-transition detection (L and QL) versions	\$1
NA	NA		Low-standby-power input-transition detection (L and QL) versions	\$2.50
40,960 to 860,160 (total), consisting of 32,768 to 688,120 (single-port cluster memory) and 8192 to 172,032 (dual-port channel memory)	4096 (channel memory), 8192 (cluster memory)	Spread-spectrum-aware PLL, built-in FIFO and dual-port arbitration logic, two registers in each I/O cell, carry-chain logic, multiple I/O standards (GTL+, HSTL, SSTL2/3, PCI, LVCMOS, LVTTTL, and others)	In-system reprogrammability, self-boot embedded flash memory, 16 product terms per macrocell, JTAG, user-\$18 to \$145 programmable bus-hold, low-power operation, simple timing model, PCI-compliant/compact-hot-swap-compatible, flexible clocking, programmable slew-rate control	
245,760 to 491,520 (total), consisting of 196,608 to 393,216 (single-port cluster memory) and 49,152 to 98,304 (dual-port channel memory)	4096 (channel memory), 8192 (cluster memory)	CDR, 8B/10B encoding/decoding, SERDES, channel bonding, transmitting/receiving PLLs, spread-aware PLLs, dual-port arbitration logic, multiple I/O standards (LVCMOS, LVTTTL, PCI, SSTL2, SSTL3, HSTL, GTL+, and others)	200 Mbps to 1.5 Gbps, 2.5-Gbps serial signaling rate, JTAG, PCI-compliant, extremely flexible clocking options, multiple standards (Fibre Channel, Gigabit Ethernet, ESCON, DVB, SMPTE, InfiniBand, SONET/SDH OC-48)	\$80 to \$350
8192 to 49,152 (dual-port channel memory)	4096	Built-in dual-port arbitration logic, two registers in each I/O cell, carry-chain logic, multiple I/O standards (PCI, LVCMOS, LVTTTL, and others)	In-system reprogrammability, 16 product terms per macrocell, JTAG, user-programmable bus-hold, low-power operation, simple timing model, PCI compliant/compact-hot-swap-compatible, flexible clocking, programmable slew-rate control	\$12 to \$28
NA	NA		Low-power, high-performance, high-reliability, user-programmable macrocell; commercial, industrial and military formats	60 cents to \$2
NA	NA	Dedicated input pins with two registers	In-System reprogrammability, 16 product terms per macrocell, JTAG, programmable bus-hold, PCI compatible, flexible clocking, simple timing model, consistent package/pinout across all densities, bus-hold, programmable slew-rate control	\$1 to \$35
NA	NA			\$2.41 to \$2.86
NA	NA			39 cents to 99 cents
NA	NA	Schmitt Trigger, programmable clock polarity		50 cents to 75 cents
NA	NA	Schmitt Trigger on all inputs, including clock		\$1.30 to \$1.63
NA	NA		3.5-nsec propagation delay, 225-MHz 5V system performance, IEEE-1149.1 scan-testable and in-system programmable	\$2.75 to \$20
NA	NA		Second-generation SuperFAST series, 3-nsec propagation delay, 300-MHz 3.3V system performance, IEEE-1149.1 scan-testable	\$1.75 to \$13.15

TABLE 2—EDN PLD DIRECTORY: REPRESENTATIVE PALs, SPLDs, AND CPLDs (CON'T)

Product line and configuration technology (antifuse, EPROM, flash, PROM, ROM, SRAM, or other)	Core operating voltages (V)	Packaging and pincount options	Macrocell count	Number of macrocells per logic block/ number of inputs to each logic block	Logic-block interconnect approach (global or hierarchical)
2000VL (EEPROM)	2.5	CABGA 49/100, FPBGA 144/208, PLCC 44, PQFP 160, TQFP 44/48/100/128/176	32 to 192	Four/18	Global
5000VE (EEPROM)	3.3	BGA 272/388, FPBGA 256/388, TQFP 100/128	128 to 512	32/68	Global
ispGAL22V10, 16V8, 20V8, 22V10 (EEPROM)	3.3 to 5	PDIP 20/24, PLCC 20/28, SSOP 28	Eight to 10	NA	Global
ispLSI 8000V (EEPROM)	3.3	BGA 272/432/492	600 to 1080	20/44	Hierarchical
ispMACH4A (EEPROM)	3.3 to 5	BGA 256, CABGA 100, FPBGA 144/256/388, PLCC 44, PQFP 100/208, TQFP 44/48/100/144	32 to 512	16/36	Global
STMicroelectronics PSD4256G2(V)	3 to 3.6 or 5 to 5.5	TQFP 80	24 (input), 16 (output)	NA	Hierarchical
PSD854F2(V)	3 to 3.6 or 5 to 5.5	PLCC 52, TQFP 52	24 (input), 16 (output)	NA	Hierarchical
Xilinx CoolRunner XPLA3 (EEPROM)	2.7 to 3.6	CS 48/56/144/280, FG 324, FT 256, PC 44, PQ 208, TQ 144, VQ 44/100	32 to 384	16/36	Global
XC9500 (flash)	4.75 to 5.25	BG 352, CS 48, HQ 208, PC 44/84, PQ 100/160, TQ 100/144, VQ 44	36 to 288	18/36	Global
XC9500XL (flash)	3 to 3.6	BG 256, CS 48/144/280, FG 256, PC 44, PQ 208, TQ 100/144, VQ 44/64	36 to 288	18/54	Global
XC9500XV (flash)	2.4 to 2.6	CS 48/144/280, FG 256, PC 44, PQ 208, TQ 100/144, VQ 44	36 to 288	18/54	Global

Note: Information in this table, including pricing, comes directly from the vendors. Please confirm information before finalizing your design.

and in-system programmable

Embedded memory density (bits)	Size of each embedded memory block (bits)	Other embedded functions	Other notable features	Price range (end of 2001; 10,000 units; cheapest package; lowest speed; commercial temperature)
NA	NA		5-nsec propagation delay, 180-MHz 2.5V system performance, IEEE-1149.1 scan-testable and in-system programmable	\$1.95 to \$15.25
NA	NA		Second generation SuperWide series, pin-by-pin-selectable 3.3 or 2.5V I/O buffers, 5-nsec propagation delay, 180-MHz 3.3V system performance, IEEE-1149.1 scan-testable and in-system programmable	\$9.25 to \$68
NA	NA		3.5- to 4-nsec propagation delay, 250 MHz, in-system programmable	83 cents to \$3.68
NA	NA		Internal tristate buses, user-selectable 3.3 or 2.5V I/O buffers, IEEE-1149.1 scan-testable and in-system programmable	\$56 to \$90
NA	NA		Guaranteed fixed timing to 20 product terms, 5-nsec propagation delay, 182-MHz system performance, IEEE-1149.1 scan-testable and in-system programmable	\$1 to \$46
9,175,040	524,288 and 8,388,608 (flash) and 262,144 (SRAM)	Microcontroller interface, JTAG ISP, memory-decode PLD	Connects to any CISC microcontroller with a 16-bit external bus; microcontroller can directly access each macrocell	\$10.13
4,718,592	262,144 and 4,194,304 (flash) and 262,144 (SRAM)	Microcontroller interface, JTAG ISP, memory-decode PLD	Connects to any CISC microcontroller with an 8-bit external bus; microcontroller can directly access each macrocell	\$7.77
NA	NA	Input registers	Ultralow power consumption, high performance, local clock inversion, multiple control signals, input hysteresis on all pins, hot-plugging capability, full IEEE-1149.1 JTAG support for ISP, slew-rate control on all outputs, high endurance	\$1.70 to \$49.05
NA	NA		High performance, superior pin-locking and routability, local clock inversion, individual output enable, input hysteresis on all pins, bus-hold circuitry on all user inputs, hot-plugging capability, full IEEE-1149.1 JTAG support for ISP, slew-rate control on all outputs, high endurance, user-programmable ground capability	\$2.85 to \$25.95
NA	NA		High performance, superior pin-locking and routability, local clock inversion, individual output enable, input hysteresis on all pins, bus-hold circuitry on all user inputs, hot-plugging capability, full IEEE-1149.1 JTAG support for ISP, slew-rate control on all outputs, high endurance, user-programmable ground capability	99 cents to \$15.50
NA	NA		High performance, superior pin-locking and routability, local clock inversion, individual output enable, input hysteresis on all pins, bus-hold circuitry on all user inputs, hot-plugging capability, full IEEE-1149.1 JTAG support for ISP, slew-rate control on all outputs, high endurance, user-programmable ground capability	\$1.15 to \$15.50